PRODUCT SPECIFICATION

6223A-SRD

Wi-Fi Single-band 1x1 + Bluetooth 2.1/4.2

Combo Module

Version:v1.9

Customer: _____

Customer P/N: _____

Signature: _____

Date: _____

Office: 14th floor, Block B, phoenix zhigu, Xixiang Street, Baoan District, Shenzhen

Factory: NO.8, Litong RD., Liuyang Economic & Technical Development Zone, Changsha, CHINA

TEL:+86-755-2955-8186 Website:www.fn-link.com

6223A-SRD Module Datasheet

Ordering Information	Part NO.	Description
	FG6223ASRD-W4	RTL8723DS, b/g/n, Wi-Fi BLE4.2, 1T1R, 12X12mm, SDIO/ Uart, PCB version V2.0, with shielding,DC-DC type(萤石版)

Target power:

2.4G: 21/15/14

CONTENTS

Revision History

Version	Date	Contents of Revision Change	Draft	Checked	Approved
V1.0	2021/08/27	New version		LXY	QJP
V1.1	2021/12/28	1.Update the specification format 2.Up and down electricity time series supplement 3.The RF index was changed to ±2dbm 4.W7&W1&W2&W4&W6 merge into a module datasheet	FC	LXY	QJP
V1.2	2022/02/07	Update power supply DC Characteristics and power consumption	FC	LXY	QJP
V1.3	2022/03/04	Modify the WIFI specification	FC	LXY	QJP
V1.4	2023/01/04	Added Truly PCB	LXY	LXY	QJP
V1.5	2023/02/09	Update timing table content Update Operating temperature	FC	LXY	QJP
V1.6	2023/11/09	Add Certificate No	Lxp	LXY	Qjp
V1.7	2024/09/14	Update Marking Description	Lxp	LXY	Qjp
V1.8	2024/10/21	Update Module Picture	Lxp	LXY	Qjp
V1.9	2024/10/31	Update Inductor Description	Lxp	LXY	Qjp

1. General Description

1.1 Introduction

6223A-SRD is a small size and low profile of Wi-Fi + BT Combo module with LGA (Land-Grid Array) footprint, board size is 12*12mm. It can be easily manufactured on SMT process and highly suitable for tablet PC, ultra book, mobile device and consumer products. It provides SDIO interface for Wi-Fi to connect with host processor and high speed UART interface for BT. It also has a PCM interface for audio data transmission with direct link to external audio codec via BT controller. The Wi-Fi throughput can go up to 150Mbps in theory by using 1x1 802.11n b/g/n SISO technology and Bluetooth can support BT2.1and BT4.2.

6223A-SRD uses highly integrated Wi-Fi/BT single chip based on advanced COMS process. integrates whole Wi-Fi/BT function blocks into a chip, such as SDIO/UART, MAC, BB, AFE, RFE, PA, EEPROM and LDO/SWR, except fewer passive components remained on PCB.

This compact module is a total solution for a combination of Wi-Fi + BT technologies. The module is specifically developed for Smart phones and Portable devices.

1.2 Description

Model Name	6223A-SRD
Product Description	Support Wi-Fi/Bluetooth functionalities
Dimension	L x W: 12 x 12 mm
Wi-Fi Interface	Support SDIO V2.0
BT Interface	UART / PCM
OS supported	Android /Linux/ Win CE /iOS /XP/WIN7/WIN10
Operating temperature	-10°C to 70°C
Storage temperature	-40°C to 85°C

2. Features

General Features

- Compatible with Bluetooth 2.1+EDR and V4.2 systems
- Enterprise level security which can apply WPA/WPA2 certification for Wi-Fi.
- Operate at ISM frequency bands (2.4GHz)
- IEEE standards support: IEEE 802.11b, IEEE 802.11g, IEEE 802.11n, IEEE 802.11d, IEEE 802.11e, IEEE 802.11h, IEEE 802.11i
- Wi-Fi 1 transmitter and 1 receiver allow data rates supporting up to 150 Mbps downstream and 150 Mbps upstream PHY rates

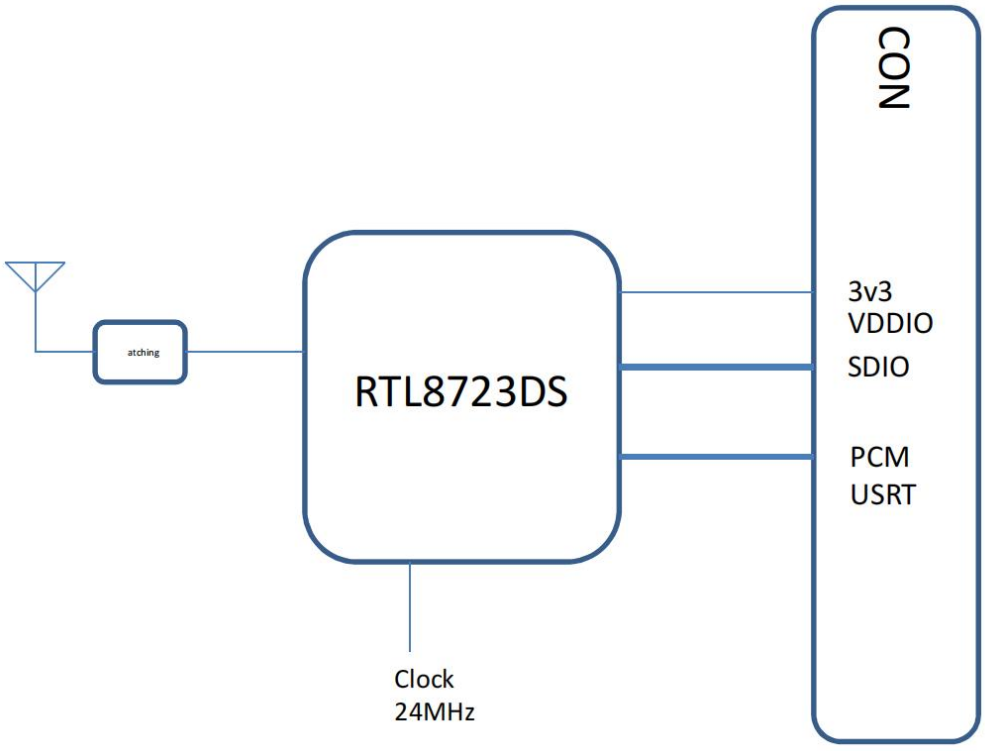
Host Interface

- SDIO for Wi-Fi and UART for Bluetooth
- PCM interface for audio data transmission via BT controller

Bluetooth Features

- Support Bluetooth 4.0 Dual mode
- Full–speed Bluetooth operation with Piconet and Scatternet support

3. Block Diagram



4. General Specification

4.1 WI-FI Specification

Feature	Description	
WLAN Standard	IEEE 802.11 b/g/n Wi-Fi compliant	
Frequency Range	2.400 GHz ~ 2.4835 GHz (2.4 GHz ISM Band)	
Number of Channels	2.4GHz：Ch1 ~ Ch14	
Test Items	**Typical Value**	**EVM**
Output Power	802.11b /11Mbps : 21dBm ± 1.5 dB	EVM ≤ -10dB
	802.11g /54Mbps : 15dBm ± 1.5 dB	EVM ≤ -25dB
	802.11n /MCS7 : 14dBm ± 1.5 dB	EVM ≤ -28dB
Spectrum Mask	Meet with IEEE standard	
Freq. Tolerance	±20ppm	
SISO Receive Sensitivity (11b,20MHz) @8% PER	- 1Mbps PER @ -91 dBm	≤-83
	- 2Mbps PER @ -89 dBm	≤-80
	- 5.5Mbps PER @ -86 dBm	≤-79
	- 11Mbps PER @ -84 dBm	≤-76
SISO Receive Sensitivity (11g,20MHz) @10% PER	- 6Mbps PER @ -87 dBm	≤-85
	- 9Mbps PER @ -86 dBm	≤-84
	- 12Mbps PER @ -84 dBm	≤-82
	- 18Mbps PER @ -82 dBm	≤-80
	- 24Mbps PER @ -79 dBm	≤-77
	- 36Mbps PER @ -75 dBm	≤-73
	- 48Mbps PER @ -71 dBm	≤-69
	- 54Mbps PER @ -70 dBm	≤-68
SISO Receive Sensitivity (11n,20MHz) @10% PER	- MCS=0 PER @ -87 dBm	≤-85
	- MCS=1 PER @ -84 dBm	≤-82
	- MCS=2 PER @ -82 dBm	≤-80
	- MCS=3 PER @ -79 dBm	≤-77
	- MCS=4 PER @ -75 dBm	≤-73
	- MCS=5 PER @ -71 dBm	≤-69
	- MCS=6 PER @ -70 dBm	≤-68
	- MCS=7 PER @ -69 dBm	≤-67
SISO Receive Sensitivity (11n,40MHz) @10% PER	- MCS=0, PER @ -84 dBm	≤-82
	- MCS=1, PER @ -81 dBm	≤-79
	- MCS=2, PER @ -79 dBm	≤-77

	- MCS=3, PER @ -76 dBm	≤-74
	- MCS=4, PER @ -72 dBm	≤-70
	- MCS=5, PER @ -68 dBm	≤-66
	- MCS=6, PER @ -67 dBm	≤-65
	- MCS=7, PER @ -66 dBm	≤-64
Maximum Input Level	802.11b : -8 dBm	
	802.11g/n : -20 dBm	
Antenna Reference	Small antennas with 0~2 dBi peak gain	

4.2 Bluetooth Specification

Feature	**Description**		
General Specification			
Bluetooth Standard	Bluetooth V4.2 of 1, 2 and 3 Mbps.		
Host Interface	UART		
Antenna Reference	Small antennas with 0~2 dBi peak gain		
Frequency Band	2400 MHz ~ 2483.5 MHz		
Number of Channels	79 channels		
Modulation	GFSK, π/4-DQPSK, 8-DPSK		
RF Specification			
	Min(dBm)	**Typical**(dBm)	**Max**(dBm)
Output Power (Class 1)	7	10	13
Sensitivity @ BER=0.1% for GFSK (1Mbps)		-89	
Sensitivity @ BER=0.01% for π/4-DQPSK (2Mbps)		-86	
Sensitivity @ BER=0.01% for 8DPSK (3Mbps)		-83	
Maximum Input Level	GFSK (1Mbps):-20dBm		
	π/4-DQPSK (2Mbps) :-20dBm		
	8DPSK (3Mbps) :-20dBm		

5. ID setting information

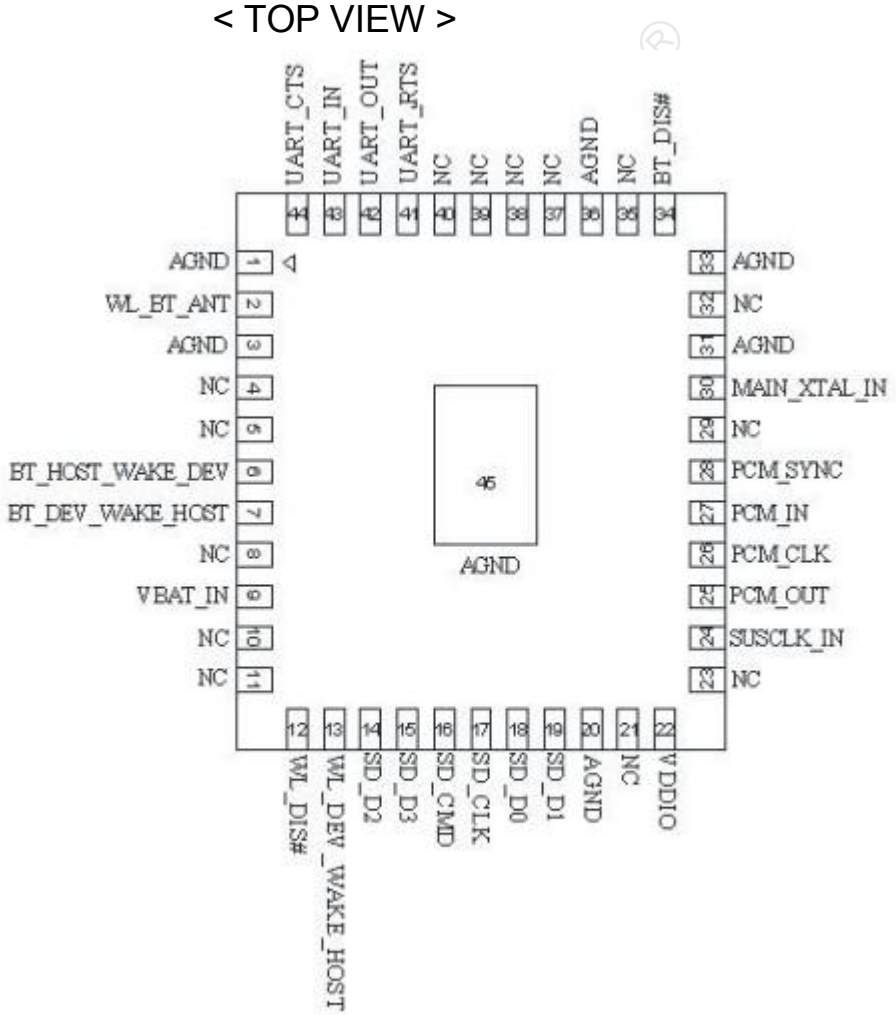
WI-FI

Vendor ID	024C
Product ID	D723

6. Pin Definition

6.1 Pin Outline

< TOP VIEW >



6.2 Pin Definition details

NO.	Name	Type	Description	Voltage
1	AGND		Ground connections	
2	WL_BT_ANT	I/O	RF I/O port	
3	AGND		Ground connections	
4	NC		Floating (NC)	
5	NC		Floating (NC)	
6	HOST_WAKE_BT	I	Host to wake up Bluetooth device	VDDIO
7	BT_WAKE_HOST	O	Bluetooth device to wake up host. (muti function for Test mode configuration. pull high to test mode ; pull low to normal mode .when wifi power on this pin must keep low)	VDDIO
8	NC		Floating (NC)	
9	VBAT_IN	P	3.3±10% V Main power voltage source input	3.3V
10	NC		Floating (NC)	
11	NC		Floating (NC)	
12	WL_DIS#	I	Pull high: ON , Pull low: OFF External pull low can disable WL	3.3V
13	WL_HOST_WAKE	O	WLAN to wake up HOST	VDDIO
14	SD_D2	I/O	SDIO data line 2	
15	SD_D3	I/O	SDIO data line 3	
16	SD_CMD	I/O	SDIO command line	
17	SD_CLK	I	SDIO clock line	
18	SD_D0	I/O	SDIO data line 0	
19	SD_D1	I/O	SDIO data line 1	
20	AGND		Ground connections	
21	NC		Floating(NC)	
22	VDDIO	P	I/O Voltage supply input	VDDIO
23	NC		Floating (NC)	
24	SUSCLK_IN	I	External Clock input(32.768kHz). Can keep NC.	
25	PCM_OUT	O	PCM Output	VDDIO
26	PCM_CLK	I/O	PCM Clock	VDDIO
27	PCM_IN	I	PCM Input	VDDIO
28	PCM_SYNC	O	PCM Sync	VDDIO
29	NC		Floating (NC)	
30	MAIN_XTAL_IN	O	Floating (NC)	
31	AGND		Ground connections	

32	NC		Floating (NC)	
33	AGND		Ground connections	
34	BT_DIS#	I	Pull high: ON , Pull low: OFF External pull low can disable BT	3.3V
35	NC		Floating (NC)	
36	AGND		Ground connections	
37	NC		Floating (NC)	
38	NC		Floating (NC)	
39	NC		Floating (NC)	
40	NC		Floating (NC)	
41	UART_RTS		UART RTS, module side is Ground connections	
42	UART_OUT	O	UART Output	VDDIO
43	UART_IN	I	UART Input	VDDIO
44	UART_CTS	I	UART CTS,	VDDIO
45	AGND		Floating (NC)	

P:POWER I:INPUT O:OUTPUT VDDIO:3.3V

7. Electrical Specifications

7.1 Power Supply DC Characteristics

The digital IO supports VDD33 or VDD18 application.

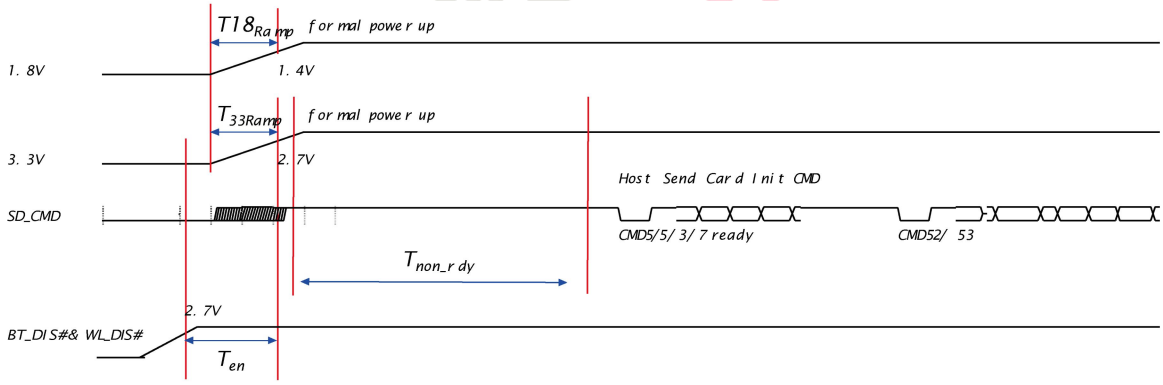
	MIN	TYP	MAX	Unit
Operating Temperature	-10	25	70	deg.C
VCC33	3.0	3.3	3.6	V
VDDIO	1.62	1.8 or 3.3	3.6	V

7.2 Power Consumption

Power Consumption (Typical by using SWR)	Wi-Fi only: TX b mode 20MHz: 335 mA (max) RX b mode 20MHz: 80 mA (max) TX n mode 40MHz: 133 mA (max) RX n mode 40MHz: 53 mA (max) TX n mode 20MHz: 137 mA (max) RX n mode 20MHz: 47 mA (max) BT: TX: 101.8 mA (max) RX: 75.8 mA (max) IDEL: 50.5 mA (max)

7.3 SDIO Power-on sequence

After power-on, the SDIO interface is selected by the RTL8723DS automatically when a valid SDIO command is received. To attain better SDIO host compatibility, the following power-on sequence is recommended.



Symbol	Description
T_{33ramp}	The 3.3V main power ramp up duration.
T_{18ramp}	The 1.8V main power ramp up duration.
T_{non_rdy}	SDIO Not Ready Duration. In this state, the RTL8723DS may respond to commands without the ready bit being set. After the ready bit is set, the host will initiate complete card detection procedure.
T_{en}	Interval between the rising point of 3.3V and WL_DIS#& BT_DIS# pull up with WL_DIS#& BT_DIS function enabled.

After main 3.3V ramp up and 1.8V ramp up, the power management unit is enabled by the power ready detection circuit. The power management unit enables the SDIO block. eFUSE is then autoloaded to SDIO circuits during the Tnon_rdy duration. After CMD5/5/3/7 procedures, card detection is executed. When the driver has loaded, normal CMD52 and CMD53 are used.

	Min	Typical	Max	Unit
T33ramp	0.2	0.5	2.5	ms
T18ramp	0.2	0.5	2.5	ms
Tnon-rdy	1	2	10	ms
T_{en}	-	0	-	ms

7.4 Interface Circuit time series

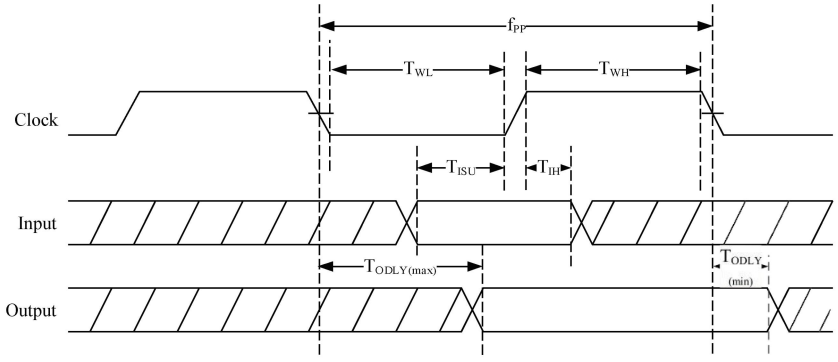
7.4.1 SDIO Pin Description

The module supports SDIO v2.0 signal level ranges form 1.8V to 3.3V.

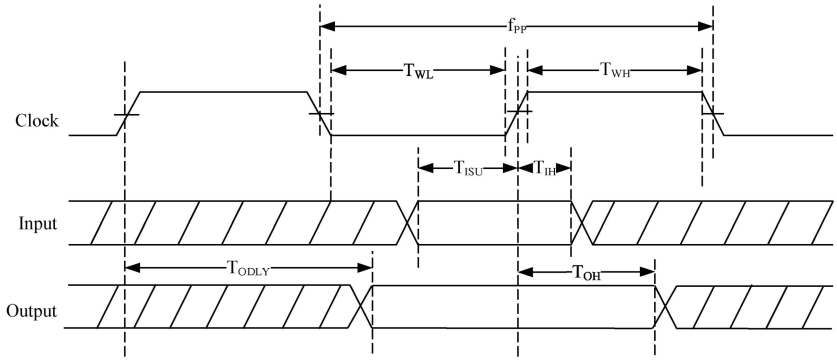
SDIO Pin Description

SD 4-Bit Mode	
DATA0	Data Line 0
DATA1	Data Line 1 or Interrupt
DATA2	Data Line 2 or Read Wait
DATA3	Data Line 3
CLK	Clock
CMD	Command Line

7.4.2 SDIO Timing table



SDIO Interface Timing

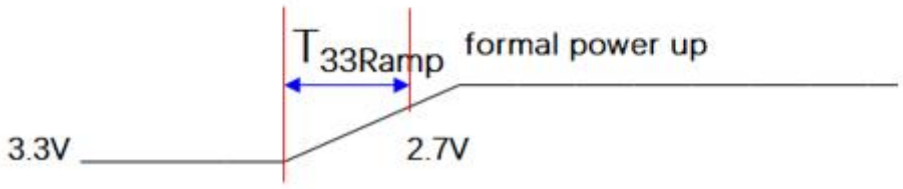


SDIO High Speed Interface Timing

NO	Parameter	Mode		MIN	MAX	Unit
f_{PP}	Clock Frequency	DEF		0	25	MHz
		HS		0	50	MHz
T_{WL}	Clock Low Time	DEF		10	-	ns
		HS		7	-	ns
T_{WH}	Clock High Time	DEF		10	-	ns
		HS		7	-	ns
T_{ISU}	Input Setup Time	DEF		5	-	ns
		HS		6	-	ns
T_{IH}	Input Hold Time	DEF		5	-	ns
		HS		2	-	ns
T_{ODLY}	Output Delay Time	DEF	During Data Transfer Mode	-	14	ns
			During Identification Mode	-	50	
		HS		-	14	ns
NO	**Parameter**	**Mode**		**MIN**	**MAX**	**Unit**
T_{OH}	Output Hold Time	HS		2.5	-	ns

7.4.3 module power-on&off time sequence

	Min	Typical	Max	Unit
T33 power on ramp	0.2	0.5	2.5	ms
T33 power off ramp	0.2	5	10	ms



Note:

1.上下电时序请满足表格要求；

The power up ramp and power down ramp must meet the following table.

2.上下电过程如有较长时间中间电压停留都会有几率导致 efuse 被窜写；

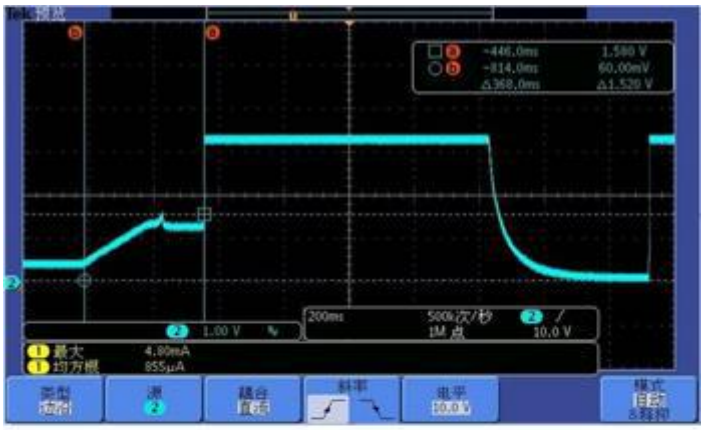
If climbing process for a long time during power-on and power-off , It may cause efuse to be overwritten.

3.建议主芯片上电完成后，再给模组上电；

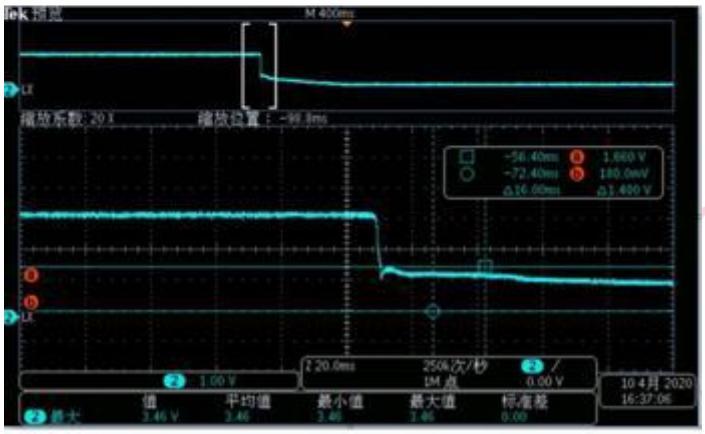
it is recommended to power on the module after platform side.

4.如有下图所示异常上下电时序，务必做相应调整符合时序规格；

If power on/off timing as below shown, must modify to meet the timing specification.



异常上电时序



异常下电时序

7.4.4 PCM interafce

Symbol	Type	Pin NO	Description
PCM IN	I	27	PCM data input
PCM OUT	O	25	PCM data output
PCM SYNC	O	28	PCM synchronization control
PCM CLK	IO	26	PCM Clock

Module supports a PCM digital audio interface that is used for transmitting digital audio/voice data to /from the audio codec.Features are supported as below:

. Support Master and slave mode

. Programmable long/short Frame sync

. Support 8-bit A-law/u-law, and 13/16-bit linear PCM format

. Support sign-extension and zero-padding for 8-bit and 13-bit samples

. Support padding of audio gain to 13-bit samples

. PCM master clock output:64,128,256,or512KHz

. Supports SCO/ESCO link

7.4.5 UART interafce

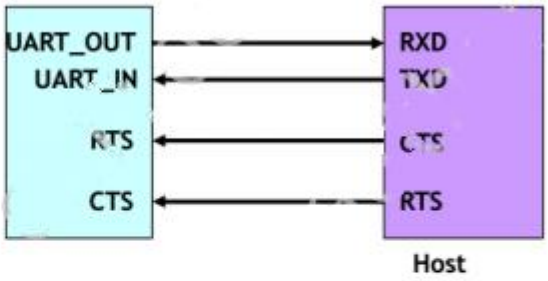
Below shown the UART hci interface connection guide.

Uart signal level ranges from 1.8V to 3.3V. must meet with the VDDIO voltage level.

HCI 硬件流程控制管脚连接

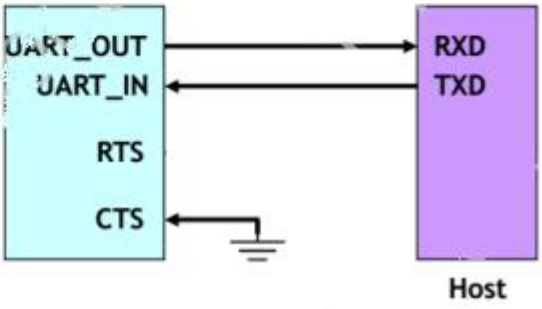
■ Host 有支持硬件流程控制的接法

圖(一)



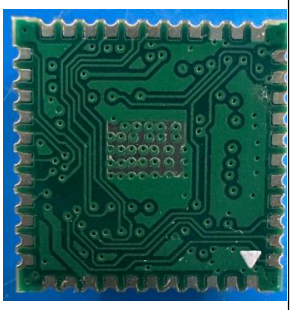
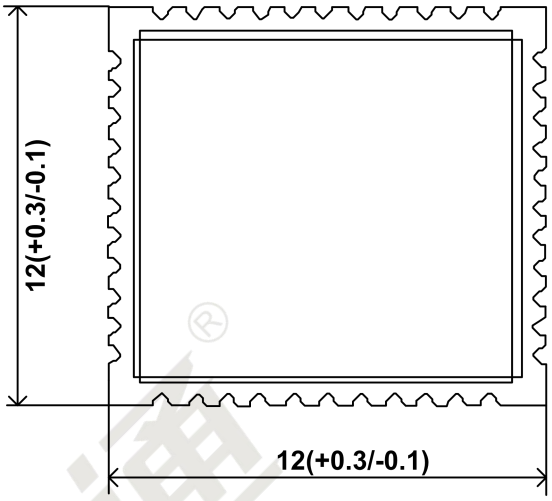
■ Host 不支持硬件流程控制的接法

圖(二)



8. Size reference

8.1 Module Picture

L x W : 12 x 12 (+0.3/-0.1) mm  	
H: 2.1 (±0.2) mm	
Weight	0.54g

8.2 Marking Description

< TOP VIEW >

二维码内容：112233445566;FG6223ASRD-W4

1. Fn-Link 商标 logo
2. 机型：6223A-SRD
3. 二维码：编码规则为“wifi mac;成品料号”

例如：112233445566;FG6223ASRD-W4（MAC 地址以实际为准）

-----BT MAC 在 WIFI MAC 基础上+1（WIFI 地址需跳 1，不能与 BT 地址重复），二维码中不显示此内容。

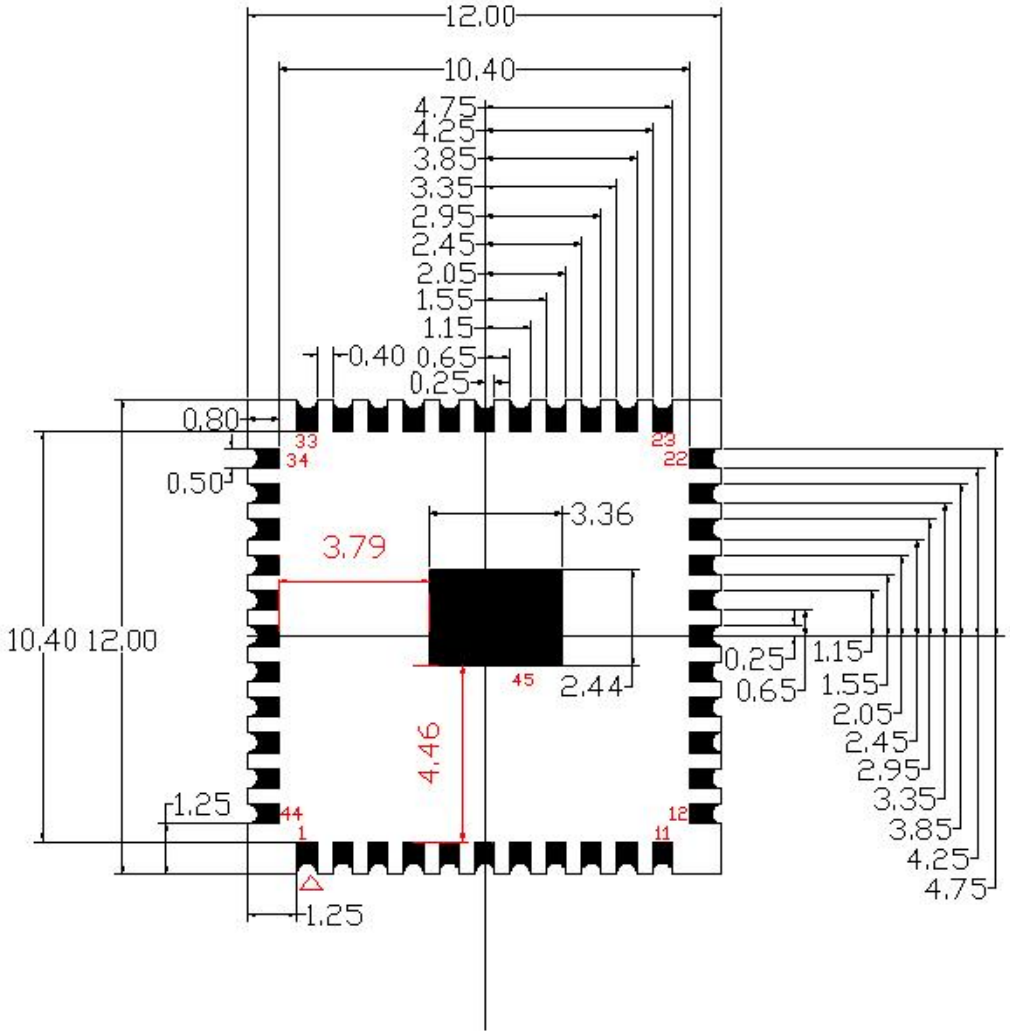
4.V/N　W4（V/N 到 W4 之间是两个空格，W4 为成品料号后缀，与二维码右对齐。）

8.3 List of certified information

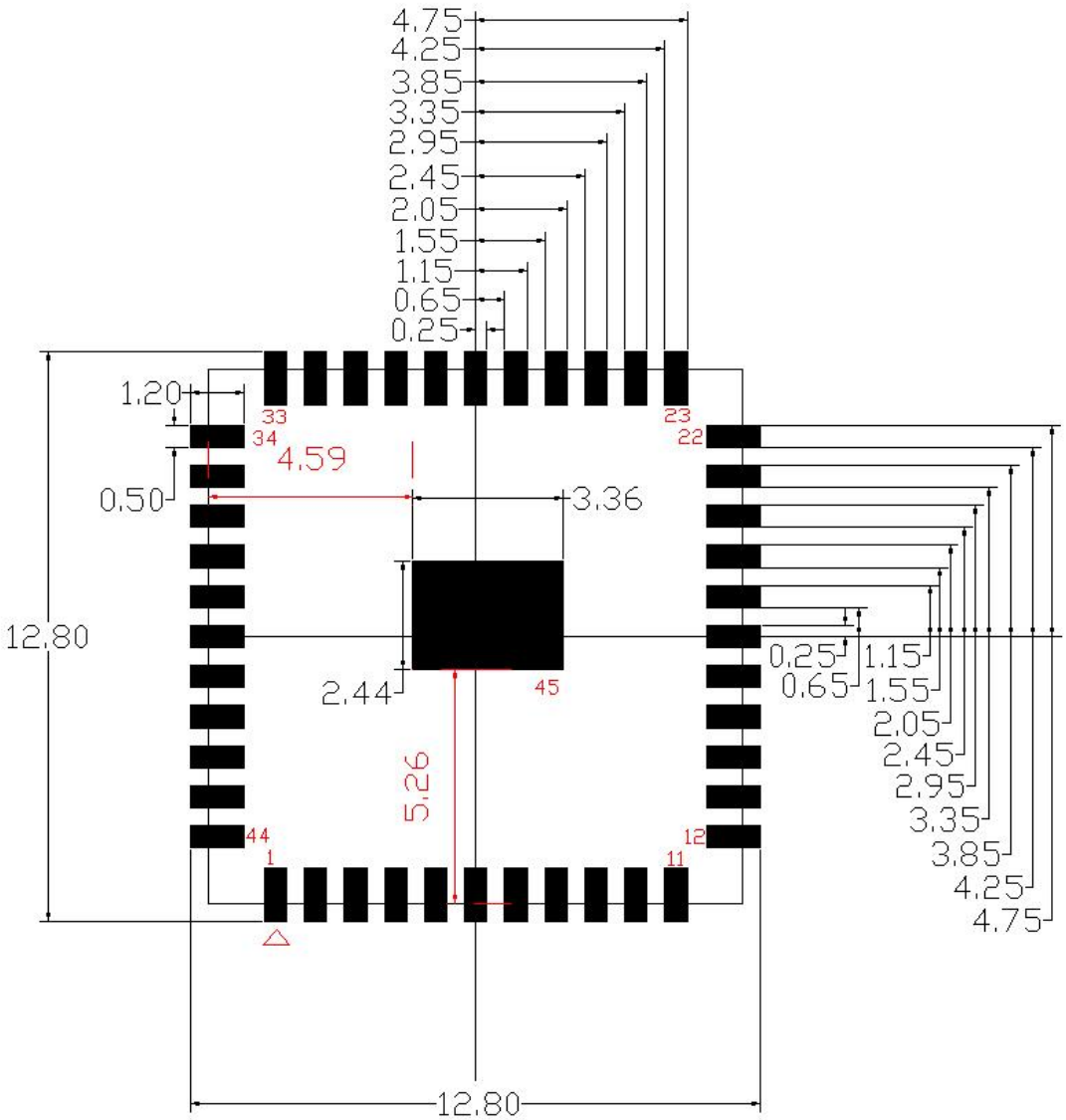
Certification project	Certificate number
SRRC	CMIIT ID:2017DP6668(M)
FCC	2AATL-6223A-SRD
CE	EC2009013S01
IC	24844-6223ASRD
NCC	TBD
KCC	R-R-Ozt-6223A-SRD
TELEC	R210-145946
Brazil	TBD
Argentina	TBD
Japan	TBD
BQB	D049930

8.4 Physical Dimensions

<TOP View>



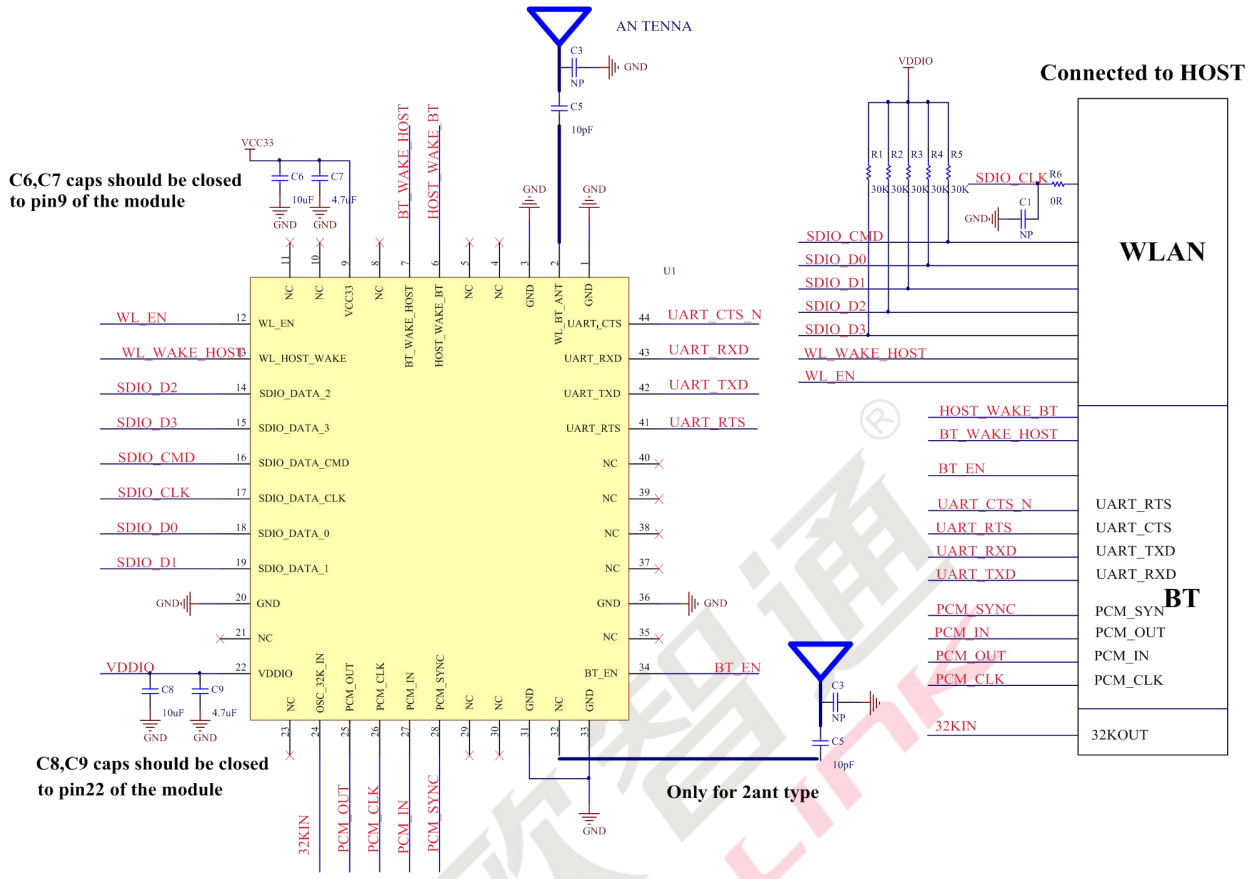
8.5 Layout Recommendation



9. The Key Material List

Item	Part Name	Description	Manufacturer
1	Chipset	RTL8723DS-CG QFN48 4.4X4.4mm	Realtek
2	PCB	6223A-SRD 12X12mm 4L	XY-PCB,KX-PCB,SL-PCB,Sunlord, Truly
3	Crystal	2520 24MHz 12pF 10ppm	TST,HOSONIC,TKD,ECEC,JWT
4	Inductor	0603 2.2uH ,±20%，Isat/rms>250/850mA	Microgate,sunlord,cenke,ceaiya
5	Shielding	6223A-SRD shielding	信太,精力通,卓益

10. Reference Design

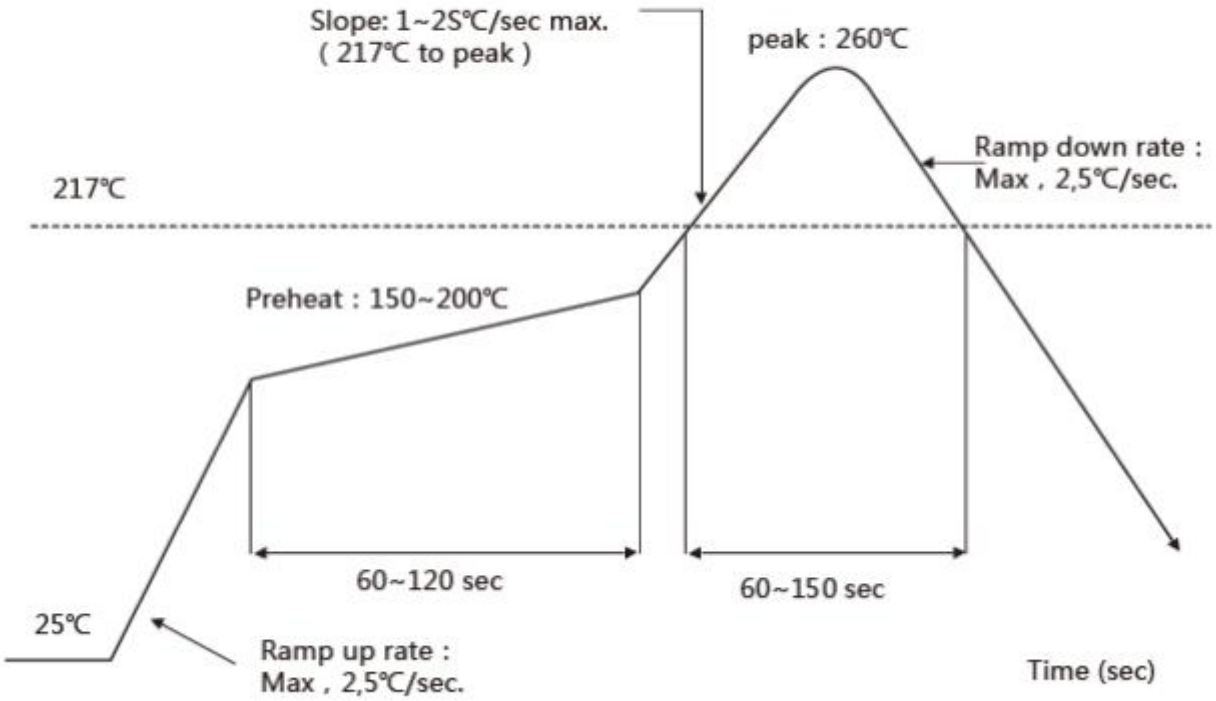


11. Recommended Reflow Profile

Referred to IPC/JEDEC standard.

Peak Temperature : <260°C

Number of Times : ≤2 times



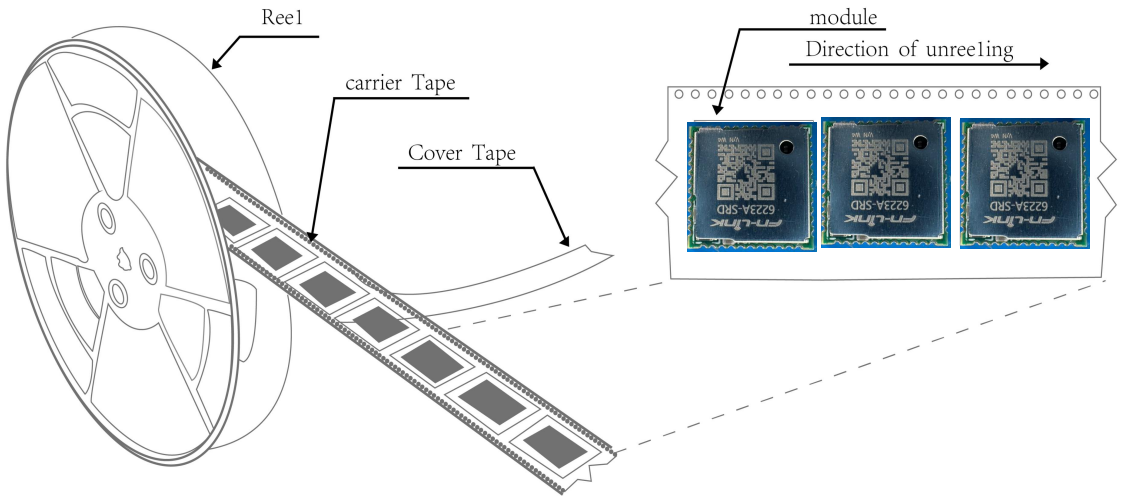
12. RoHS compliance

All hardware components are fully compliant with EU RoHS directive

13. Package

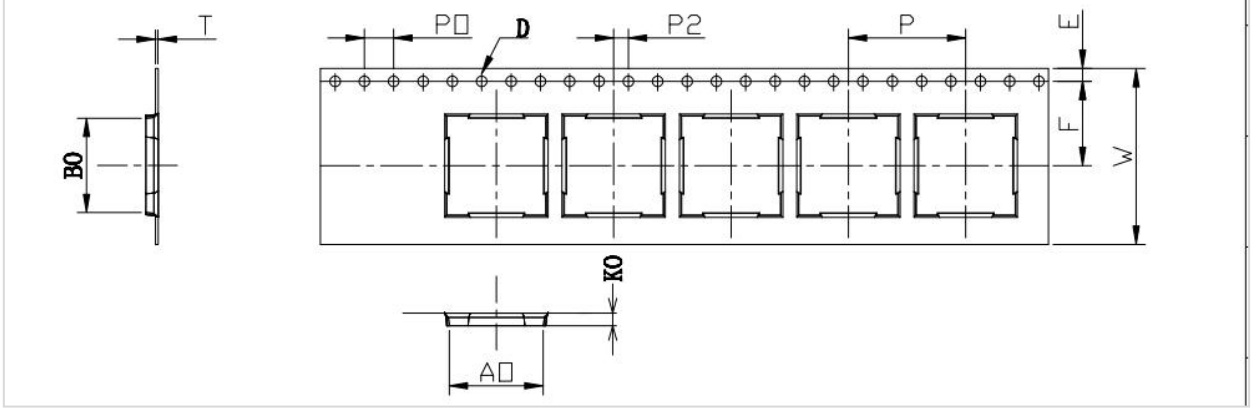
13.1 Reel

A roll of 1500pcs



13.2 Carrier Tape Detail

ITEM	W	A0	B0	D	F	E	K0	P0	P2	P	T
DIM	24	12.45	12.45	1.50	11.5	1.75	2.60	4.0	2.0	16.0	0.30
TOLE	+0.3 −0.3	±0.10	±0.10	+0.1 −0.0	+0.1 −0.1	±0.1	±0.10	±0.1	±0.1	±0.1	±0.05



13.3 Packaging Detail

the take-up package

Using self-adhesive tape

Size of black tape: 24mm*32.6m the cover tape :21.3mm*32.6m

Color of plastic disc: blue

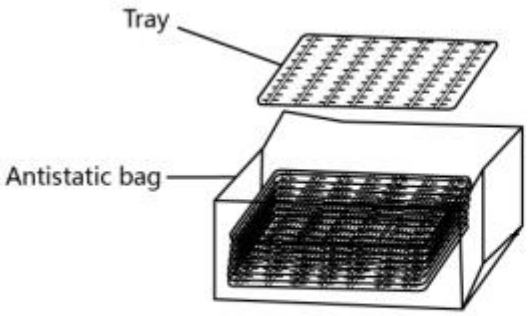
NY bag size:460mm*385mm

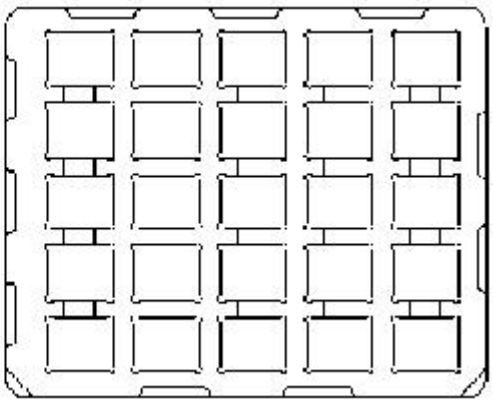
size ： 350*350*35mm

The packing case size:350*210*370mm

13.4 Tray

Use pallet packaging for less than 300 pieces





14. Moisture sensitivity

The Modules is a Moisture Sensitive Device level 3, in according with standard IPC/JEDEC J-STD-020, take care

all the relatives requirements for using this kind of components.

Moreover, the customer has to take care of the following conditions:

a) Calculated shelf life in sealed bag: 12 months at <40°C and <90% relative humidity (RH)

b) Environmental condition during the production: 30°C / 60% RH according to IPC/JEDEC J-STD-033A paragraph 5

c) The maximum time between the opening of the sealed bag and the reflow process must be 168 hours if condition

d) "IPC/JEDEC J-STD-033A paragraph 5.2" is respected

e) Baking is required if conditions b) or c) are not respected

f) Baking is required if the humidity indicator inside the bag indicates 10% RH or more