

PRODUCT SPECIFICATION

L287B-SR

Wi-Fi Dual-band 1x1 11a/b/g/n/ac+ Bluetooth 5.2

Combo Module

Version:v2.1



L287B-SR Module Datasheet

Ordering Information	Part NO.	Description
	FGL287BSRX-01	88W8987-A2-NYEE, a/b/g/n/ac, Wi-Fi, BT5.2, 1T1R, SDIO+UART, 2 Antenna version, PCB V2.0, 13x15mm

Customer: _____

Customer P/N: _____

Signature: _____

Date: _____

Office: 14th floor, Block B, phoenix zhigu, Xixiang Street, Baoan District, Shenzhen

Factory: NO.8, Litong RD., Liuyang Economic & Technical Development Zone, Changsha, CHINA

TEL:+86-755-2955-8186

Website:www.fn-link.com

CONTENTS

1. General Description	5
1.1 Introduction	5
1.2 Description	5
2. Features	6
3. Block Diagram	6
4. General Specification	7
4.1 2.4GHz RF Specification	7
4.2 5GHz RF Specification	8
4.3 Bluetooth Specification	10
5. Pin Definition	11
5.1 Pin Outline	11
5.2 Pin Definition details	11
6. Electrical Specifications	13
6.1 Power Supply DC Characteristics	13
6.2 Power Consumption	14
6.3 Power-up sequence	15
6.4 Interface Circuit time series	15
6.4.1 SDIO Default Speed, High Speed Mode Timing	15
6.4.2 SDIO SDR12, SDR25, SDR50 modes (up to 100 MHz) (1.8V)	16
6.4.3 SDIO SDR104 mode (208 MHz) (1.8V)	17
6.4.4 SDIO DDR50 mode (50 MHz) (1.8V)	18
6.4.5 High-speed UART specifications	19
6.4.6 Bluetooth PCM Timing	20
7. Size reference	22
7.1 Module Picture	22
7.2 Marking Description	22
7.3 List of certified information	23
7.4 Physical Dimensions	24
7.5 Layout Recommendation	25
8. The Key Material List	25
9. Reference Design	26
10. Recommended Reflow Profile	27
11. Package	27
11.1 Reel	27
11.2 Carrier Tape Detail	28
11.3 Packaging Detail	29
12. Moisture sensitivity	29

Revision History

[illegible]

1. General Description

1.1 Introduction

L287B-SR has dual-band Wi-Fi and Bluetooth functionalities. It is based on NXP 88W8987 chipset, a highly-integrated IEEE 802.11a/b/g/n/ac MAC/Baseband/Rf WLAN and Bluetooth Baseband/Rf single chip. The module provides SDIO3.0 interface for Wi-Fi and HS-UART/PCM for Bluetooth.

L287B-SR can achieve up to a speed of 433.3Mbps with single stream 802.11ac WLAN connection. It is a perfect solution for a combination of Wi-Fi and BT technologies.

1.2 Description

Model Name	L287B-SR
Product Description	Support Wi-Fi/Bluetooth functionalities
Dimension	L x W x H: 15 x 13 x 2.15 mm (typical)
Wi-Fi Interface	Support SDIO3.0
BT Interface	UART / PCM
OS supported	Android /Linux/ Win CE/XP/WIN7/WIN10
Operating temperature	-30°C to 85°C
Storage temperature	-40°C to 125°C

[Note] For FGL287BSRX-01, Baud-rate of UART interface is 115200 by default.

2. Features

General Features

- NXP 88W8987 inside
- Supports link layer topology to be master and slave (connects up to 16 links)
- Wi-Fi/Bluetooth coexistence protocol support

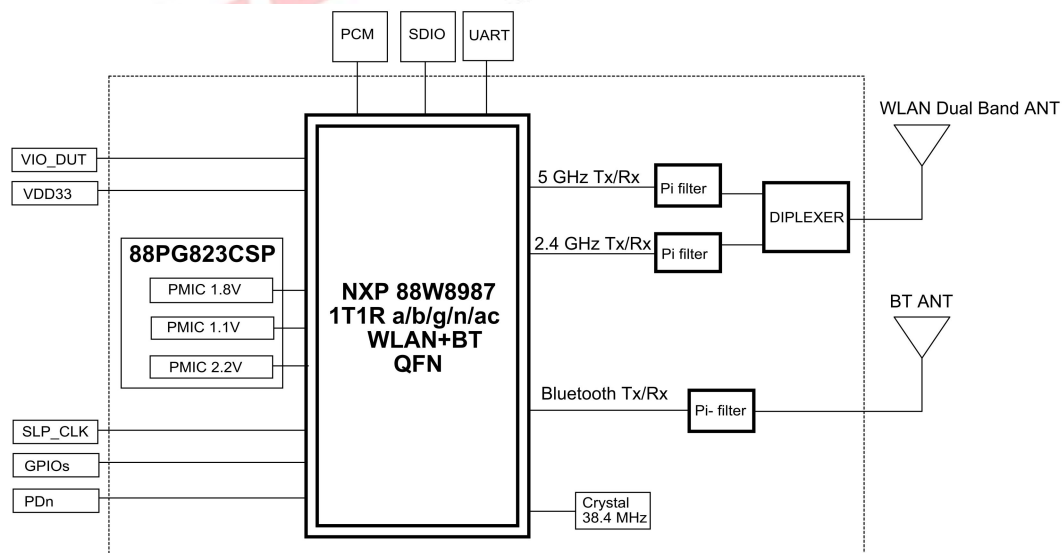
WLAN Features

- SDIO3.0 interface for WLAN
- CMOS MAC, Baseband PHY and RF in a single chip for IEEE 802.11 a/b/g/n/ac
- Support 802.11ac, 1x1 with data rates up to MCS9
- Maximum rate 433Mbps in 80MHz bandwidth

Bluetooth Features

- Support Bluetooth V5.2 features
- HS-UART and PCM interface for BT
- Bluetooth LE supports Broadcaster, Observer, Central, and Peripheral roles

3. Block Diagram



4. General Specification

4.1 2.4GHz RF Specification

Feature	Description	
WLAN Standard	IEEE 802.11 b/g/n Wi-Fi compliant	
Frequency Range	2.400 GHz ~ 2.4835 GHz (2.4 GHz ISM Band)	
Number of Channels	2.4GHz: Ch1 ~ Ch14	
Test Items	Typical Value	EVM
Output Power	802.11b /11Mbps : 17dBm $\pm$ 2 dB	EVM $\leq$ -9dB
	802.11g /54Mbps : 15dBm $\pm$ 2 dB	EVM $\leq$ -25dB
	802.11n /MCS7 : 14dBm $\pm$ 2 dB	EVM $\leq$ -28dB
Spectrum Mask	Meet with IEEE standard	
Freq. Tolerance	$\pm$ 20ppm	
Test Items	TYP Test Value	Standard Value
SISO Receive Sensitivity (11b,20MHz) @8% PER	- 1Mbps $\leq$ -92 dBm	$\leq$ -85 dBm
	- 11Mbps $\leq$ -82 dBm	$\leq$ -76 dBm
SISO Receive Sensitivity (11g,20MHz) @10% PER	- 6Mbps $\leq$ -86 dBm	$\leq$ -82 dBm
	- 54Mbps $\leq$ -71 dBm	$\leq$ -65 dBm
SISO Receive Sensitivity (11n,20MHz) @10% PER	- MCS=0 $\leq$ -86 dBm	$\leq$ -82 dBm
	- MCS=7 $\leq$ -67 dBm	$\leq$ -64 dBm
SISO Receive Sensitivity (11n,40MHz) @10% PER	- MCS=0 $\leq$ -83 dBm	$\leq$ -79 dBm
	- MCS=7 $\leq$ -65 dBm	$\leq$ -61 dBm
Maximum Input Level	802.11b : -10 dBm	
	802.11g/n : -20 dBm	

4.2 5GHz RF Specification

Feature	Description	
WLAN Standard	IEEE 802.11a/n/ac 1x1, Wi-Fi compliant	
Frequency Range	5.150 GHz ~ 5.850 GHz (5.0 GHz Band)	
Number of Channels	5.0GHz: Please see the table ¹	
Test Items	Typical Value	EVM
Output Power	802.11a /54Mbps: 15 dBm ± 2 dB	EVM ≤ -25dB
	802.11n /MCS7: 14 dBm ± 2 dB	EVM ≤ -28dB
	802.11ac	EVM ≤ -32dB
	VHT20/MCS8: 13 dBm ± 2 dB	
	VHT40/MCS9: 13 dBm ± 2 dB	
	VHT80/MCS9: 11 dBm ± 2 dB	
Test Items	Test Value	Standard Value
Receive Sensitivity (11a, 20MHz) @10% PER	- 6Mbps ≤ -86 dBm	≤ -82 dBm
	- 54Mbps ≤ -71 dBm	≤ -65 dBm
Receive Sensitivity (11n,20MHz) @10% PER	- MCS=0 ≤ -86 dBm	≤ -82 dBm
	- MCS=7 ≤ -67 dBm	≤ -64 dBm
Receive Sensitivity (11n,40MHz) @10% PER	- MCS=0 ≤ -82 dBm	≤ -79 dBm
	- MCS=7 ≤ -64 dBm	≤ -61 dBm
Receive Sensitivity (11ac,20MHz) @10% PER	- MCS=0 ≤ -85 dBm	≤ -82 dBm
	- MCS=8 ≤ -64 dBm	≤ -59 dBm
Receive Sensitivity (11ac,40MHz) @10% PER	- MCS=0 ≤ -82 dBm	≤ -79 dBm
	- MCS=9 ≤ -59 dBm	≤ -54 dBm
Receive Sensitivity (11ac,80MHz) @10% PER	- MCS=0 ≤ -79 dBm	≤ -76 dBm
	- MCS=9 ≤ -55 dBm	≤ -51 dBm
Maximum Input Level	802.11a/n: -30 dBm	

Conditions : VCC=3.3V ; VDDIO=1.8V ; Temp:25°C

¹5GHz(20MHz) Channel table

Band range	Operating Channel Numbers	Channel center frequencies (MHz)
5180MHz~5240MHz	36	5180
	40	5200
	44	5220
	48	5240
5260MHz~5320MHz	52	5260
	56	5280

	60	5300
	64	5320
5550MHz~5700MHz	100	5500
	104	5520
	108	5540
	112	5560
	116	5580
	120	5600
	124	5620
	128	5640
	132	5660
	136	5680
	140	5700
5745MHz~5825MHz	149	5745
	153	5765
	157	5785
	161	5805
	165	5825

4.3 Bluetooth Specification

Feature	Description		
General Specification			
Bluetooth Standard	Bluetooth V5.2		
Host Interface	UART		
Frequency Band	2402 MHz ~ 2480 MHz		
Number of Channels	79 channels		
Modulation	GFSK, $\pi/4$ -DQPSK, 8-DPSK		
RF Specification			
	Min(dBm)	Typical(dBm)	Max(dBm)
Output Power (BR/LE)		10	
Output Power (EDR) ^{Note1}		7	
Sensitivity @ BER=0.1% for GFSK (1Mbps) ^{Note2}		-92	
Sensitivity @ BER=0.01% for $\pi/4$ -DQPSK (2Mbps) ^{Note2}		-86	
Sensitivity @ BER=0.01% for 8DPSK (3Mbps) ^{Note2}		-85	
Maximum Input Level	GFSK (1Mbps):-20dBm		
	$\pi/4$ -DQPSK (2Mbps) :-20dBm		
	8DPSK (3Mbps) :-20dBm		

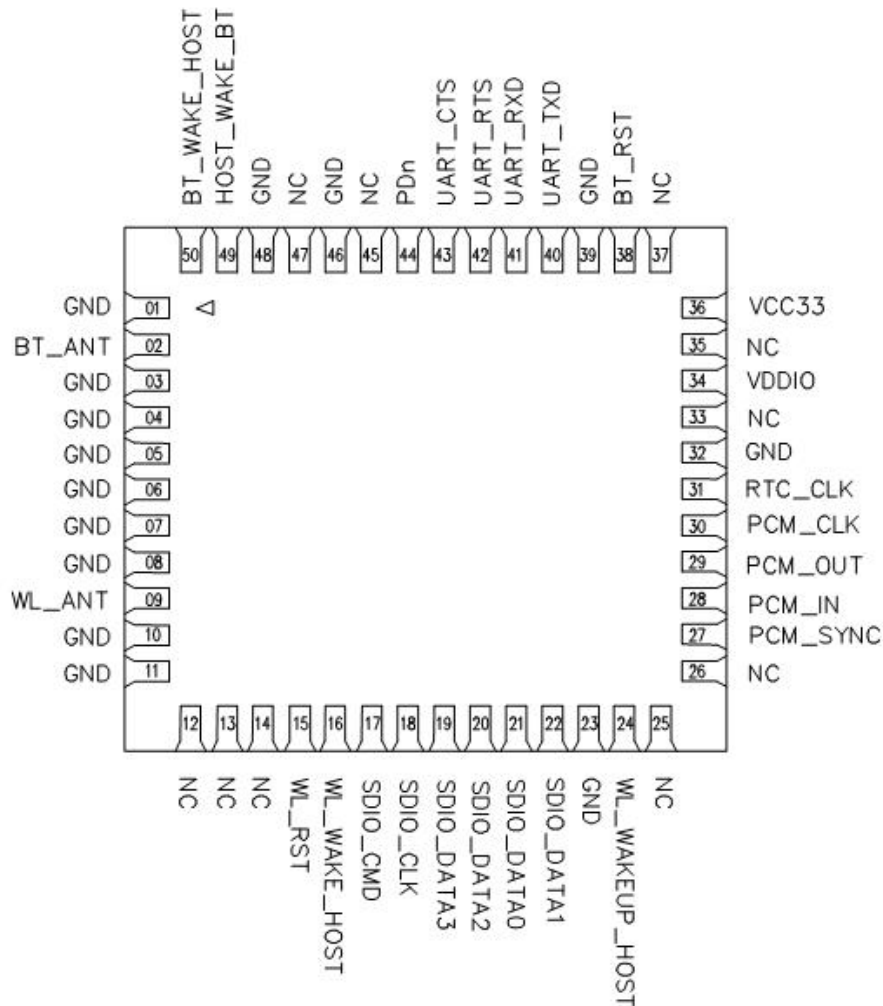
Note1: By default, 88W8987's EDR TX power is 3dBm less than BR TX power.

Note2: Desense of ~7 dB at CH 2419 MHz, ~4 dB at CH 2432 MHz, ~3 dB at 2457 MHz, ~4 dB at 2458 MHz due to internal clock harmonics of chipset.

5. Pin Definition

5.1 Pin Outline

< TOP VIEW >



5.2 Pin Definition details

NO.	Name	Type	Description	Voltage
1	GND	—	Ground connections	
2	BT_ANT	I/O	RF I/O port for BT	
3	GND	—	Ground connections	
4	GND	—	Ground connections	
5	GND	—	Ground connections	
6	GND	—	Ground connections	

7	GND	—	Ground connections	
8	GND	—	Ground connections	
9	WL_ANT	I/O	RF I/O port for dual band Wi-Fi	
10	GND	—	Ground connections	
11	GND	—	Ground connections	
12	NC	—	No connect	
13	NC	—	No connect	
14	NC	—	No connect	
15	WL_RST ^{Note1}	I	WLAN independent reset, internal pull up	1.8V
16	WL_WAKE_HOST	O	WLAN wake-up HOST, internal pull up	1.8V
17	SDIO_CMD	I/O	SDIO command line	1.8V
18	SDIO_CLK	I/O	SDIO clock line	1.8V
19	SDIO_DATA_3	I/O	SDIO data line 3	1.8V
20	SDIO_DATA_2	I/O	SDIO data line 2	1.8V
21	SDIO_DATA_0	I/O	SDIO data line 0	1.8V
22	SDIO_DATA_1	I/O	SDIO data line 1	1.8V
23	GND	—	Ground connections	
24	WL_WAKE_HOST	O	WLAN wake-up HOST, Internally short to module PIN 16	1.8V
25	NC	—	No connect	
26	NC	—	No connect	
27	PCM_SYNC	I/O	PCM sync signal	1.8V
28	PCM_IN	I	PCM data input	1.8V
29	PCM_OUT	O	PCM Data output	1.8V
30	PCM_CLK	I/O	PCM clock	1.8V
31	RTC_CLK	I	External Low Power Clock input (32.768KHz) If not used, keep NC	VDDIO
32	GND	—	Ground connections	
33	NC	—	No connect	
34	VDDIO	P	I/O Voltage supply input	1.8V
35	NC	—	No connect	
36	VCC33	P	Main power voltage source input	3.3V
37	NC	—	No connect	
38	BT_RST ^{Note1}	I	Bluetooth independent reset, internal pull up	1.8V

39	GND	—	Ground connections	
40	UART_TXD ^{Note2}	O	Bluetooth UART interface, UART_TXD must be kept low before VCC33 starts to accelerate.	1.8V
41	UART_RXD	I	Bluetooth UART interface	1.8V
42	UART_RTS_N	O	Bluetooth UART interface	1.8V
43	UART_CTS_N	I	Bluetooth UART interface	1.8V
44	PDn ^{Note3}	I	Full Power-down, active low internal pull up	1.8V to 3.3V
45	NC	—	No connect	
46	GND	—	Ground connections	
47	NC	—	No connect	
48	GND	—	Ground connections	
49	HOST_WAKE_BT	I	HOST wake-up Bluetooth device, internal pull up	1.8V
50	BT_WAKE_HOST	O	Bluetooth device to wake-up HOST, internal pull up	1.8V

P:POWER I:INPUT O:OUTPUT VDDIO:1.8V

Note1: Software reset, the host can initiate an independent reset to reload firmware. To enable this feature, customer will need to add some parameters while downloading the driver. Please contact our FAE for details.

Note2: Pin 40 is a boot up configuration pin of 88W8987, it is internally pulled low with 51KΩ, do not externally pull up.

Note3: Hardware reset, the device is reset when the PDn input pin is <0.2V and transitions from low to high, connect it to host if possible

6. Electrical Specifications

6.1 Power Supply DC Characteristics

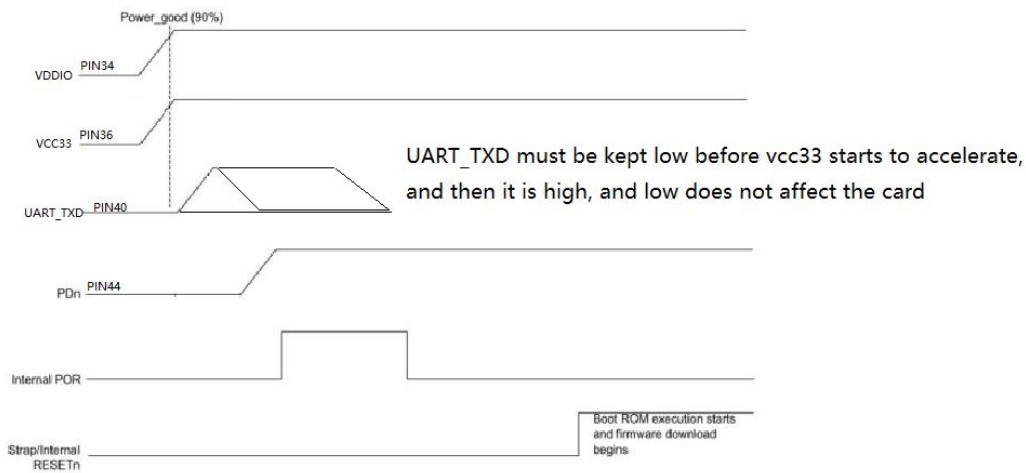
	MIN	TYP	MAX	Unit
Operating Temperature	-30	25	85	deg.C
VCC33	3.135	3.3	3.465	V
VDDIO	1.71	1.8	1.89	V

6.2 Power Consumption

[Note] The consumption is quite high while module initializing, please make sure the current supply of VCC33 power is greater than 1A.

Band	Mode		Current Consumption(Unit:mA) VCC33 = VIO = 3.3V
NA	Idle		57
2.4GHz	Continue Tx	11b 1Mbps @17dBm	483
		11g 6Mbps @17dBm	457
		11n HT20 mcs0@14dBm	475
		11n HT40 mcs0@14dBm	464
	Continue Rx	11b 1Mbps	72
		11n HT40 mcs7	72
5GHz	Continue Tx	11a 6Mbps @17.5dBm	470
		11ac VHT20 mcs0 @17dBm	492
		11ac VHT40 mcs0 @17dBm	485
		11ac VHT80 mcs0 @11dBm	292
	Continue Rx	11a 6Mbps	70
		11n HT40 mcs7	82
		11ac VHT20 mcs9	70
		11ac VHT80 mcs9	93

6.3 Power-up sequence

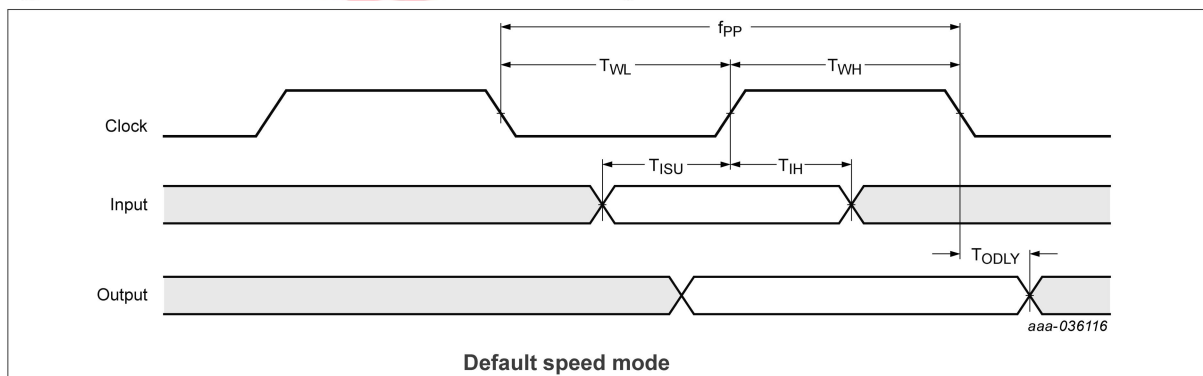


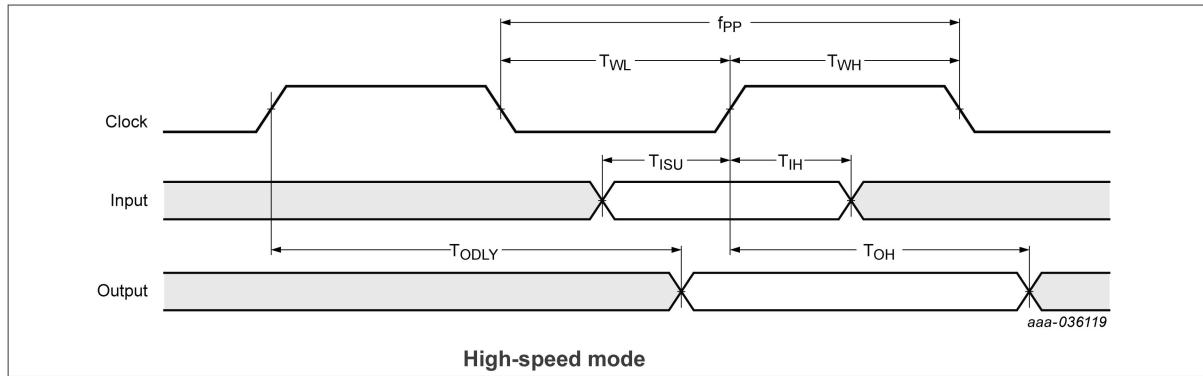
VDDIO电压必须在VCC33起来之前上升到90%的电压；或者同步上电。

- VDDIO must be good (90%) before or at the same time VCC33 starts ramping up.
- VDDIO must be good (90%) before or at the same time PDn starts ramping up.
- Ramp-up time of VDDIO must be <100 ms.
- All supplies must be monotonic.

6.4 Interface Circuit time series

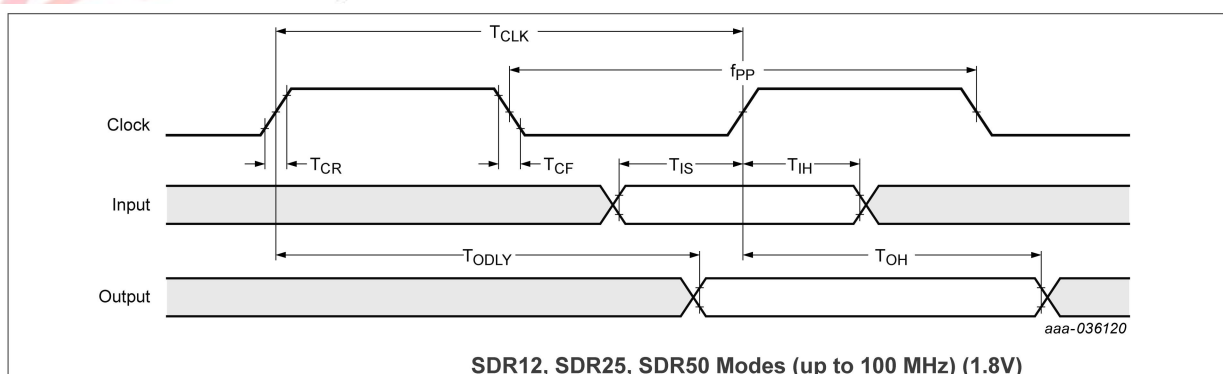
6.4.1 SDIO Default Speed, High Speed Mode Timing





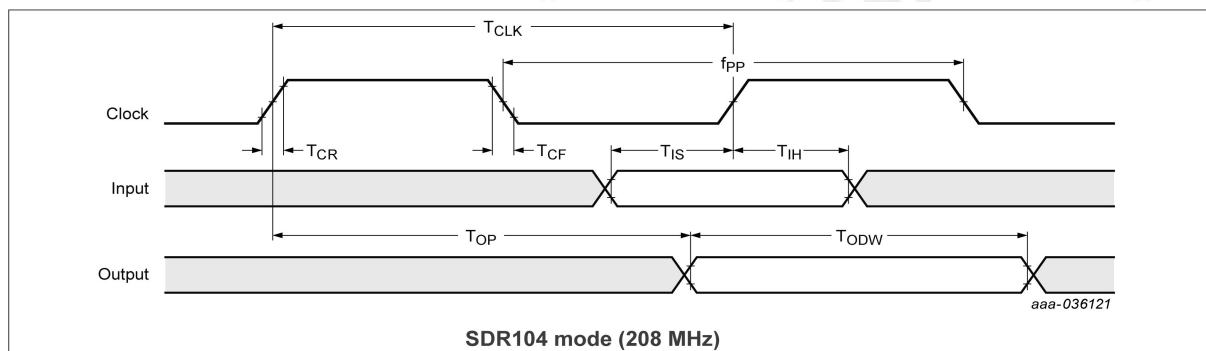
Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{PP}	Clock frequency	Normal	0	--	25	MHz
		High-speed	0	--	50	MHz
T_{WL}	Clock low time	Normal	10	--	--	ns
		High-speed	7	--	--	ns
T_{WH}	Clock high time	Normal	10	--	--	ns
		High-speed	7	--	--	ns
T_{ISU}	Input setup time	Normal	5	--	--	ns
		High-speed	6	--	--	ns
T_{IH}	Input hold time	Normal	5	--	--	ns
		High-speed	2	--	--	ns
T_{ODLY}	Output delay time	Normal	--	--	14	ns
	$CL \leq 40$ pF (1 card)	High-speed	--	--	14	ns
T_{OH}	Output hold time	High-speed	2.5	--	--	ns

6.4.2 SDIO SDR12, SDR25, SDR50 modes (up to 100 MHz) (1.8V)



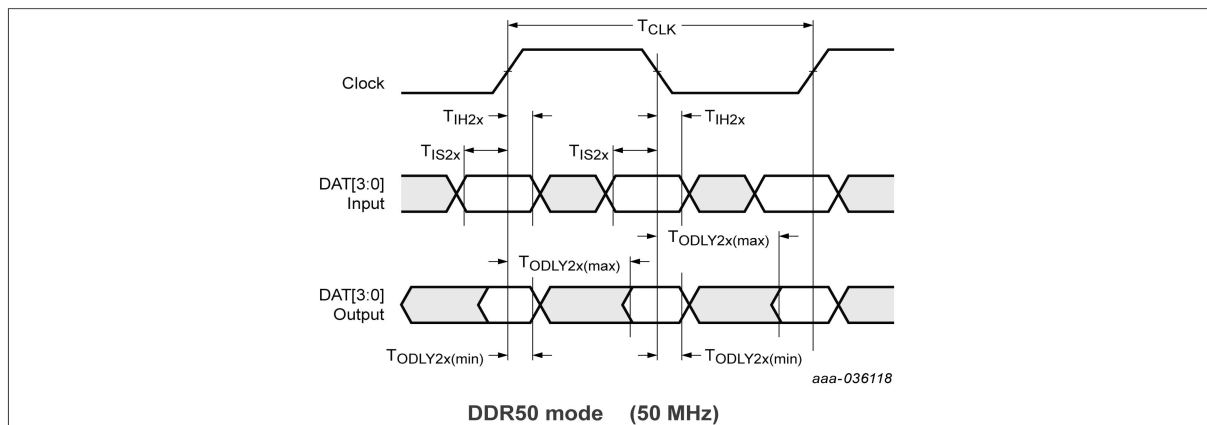
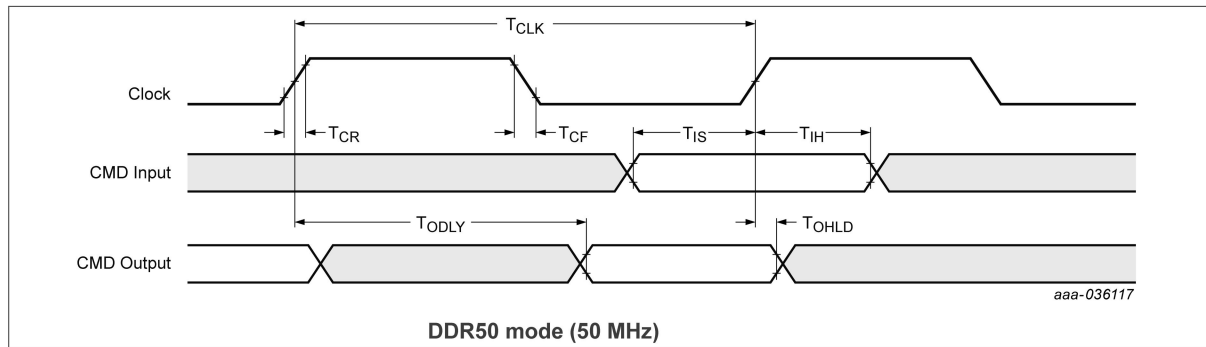
Symbol	Parameter	Condition	Min	Typ	Max	Units
f_{PP}	Clock frequency	SDR12/25/50	25	--	100	MHz
T_{IS}	Input setup time	SDR12/25/50	3	--	--	ns
T_{IH}	Input hold time	SDR12/25/50	0.8	--	--	ns
T_{CLK}	Clock time	SDR12/25/50	10	--	40	ns
T_{CR}, T_{CF}	Rise time, fall time $T_{CR}, T_{CF} < 2$ ns (max) at 100 MHz $C_{CARD} = 10$ pF	SDR12/25/50	--	--	$0.2 \cdot T_{CLK}$	ns
T_{ODLY}	Output delay time $C_L \leq 30$ pF	SDR12/25/50	--	--	7.5	ns
T_{OH}	Output hold time $C_L = 15$ pF	SDR12/25/50	1.5	--	--	ns

6.4.3 SDIO SDR104 mode (208 MHz) (1.8V)



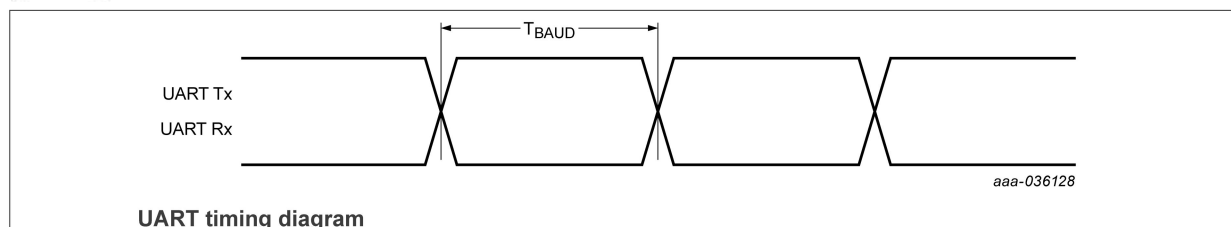
Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{PP}	Clock frequency	SDR104	0	--	208	MHz
T_{IS}	Input setup time	SDR104	1.4	--	--	ns
T_{IH}	Input hold time	SDR104	0.8	--	--	ns
T_{CLK}	Clock time	SDR104	4.8	--	--	ns
T_{CR}, T_{CF}	Rise time, fall time $T_{CR}, T_{CF} < 0.96$ ns (max) at 208 MHz $C_{CARD} = 10$ pF	SDR104	--	--	$0.2 \cdot T_{CLK}$	ns
T_{OP}	Card output phase	SDR104	0	--	10	ns
T_{ODW}	Output timing of variable data window	SDR104	2.88	--	--	ns

6.4.4 SDIO DDR50 mode (50 MHz) (1.8V)



Symbol	Parameter	Condition	Min	Typ	Max	Units
Clock						
T_{CLK}	Clock time 50 MHz (max) between rising edges	DDR50	20	--	--	ns
T_{CR}, T_{CF}	Rise time, fall time $T_{CR}, T_{CF} < 4.00$ ns (max) at 50 MHz $C_{CARD} = 10$ pF	DDR50	--	--	$0.2 \cdot T_{CLK}$	ns
Clock Duty	--	DDR50	45	--	55	%
CMD Input (referenced to clock rising edge)						
T_{IS}	Input setup time $C_{CARD} \leq 10$ pF (1 card)	DDR50	6	--	--	ns
T_{IH}	Input hold time $C_{CARD} \leq 10$ pF (1 card)	DDR50	0.8	--	--	ns
CMD Output (referenced to clock rising edge)						
T_{ODLY}	Output delay time during data transfer mode $C_L \leq 30$ pF (1 card)	DDR50	--	--	13.7	ns
T_{OHLd}	Output hold time $C_L \geq 15$ pF (1 card)	DDR50	1.5	--	--	ns
DAT[3:0] Input (referenced to clock rising and falling edges)						
T_{IS2x}	Input setup time $C_{CARD} \leq 10$ pF (1 card)	DDR50	3	--	--	ns
T_{IH2x}	Input hold time $C_{CARD} \leq 10$ pF (1 card)	DDR50	0.8	--	--	ns
DAT[3:0] Output (referenced to clock rising and falling edges)						
$T_{ODLY2x} \text{ (max)}$	Output delay time during data transfer mode $C_L \leq 25$ pF (1 card)	DDR50	--	--	7.0	ns
$T_{ODLY2x} \text{ (min)}$	Output hold time $C_L \geq 15$ pF (1 card)	DDR50	1.5	--	--	ns

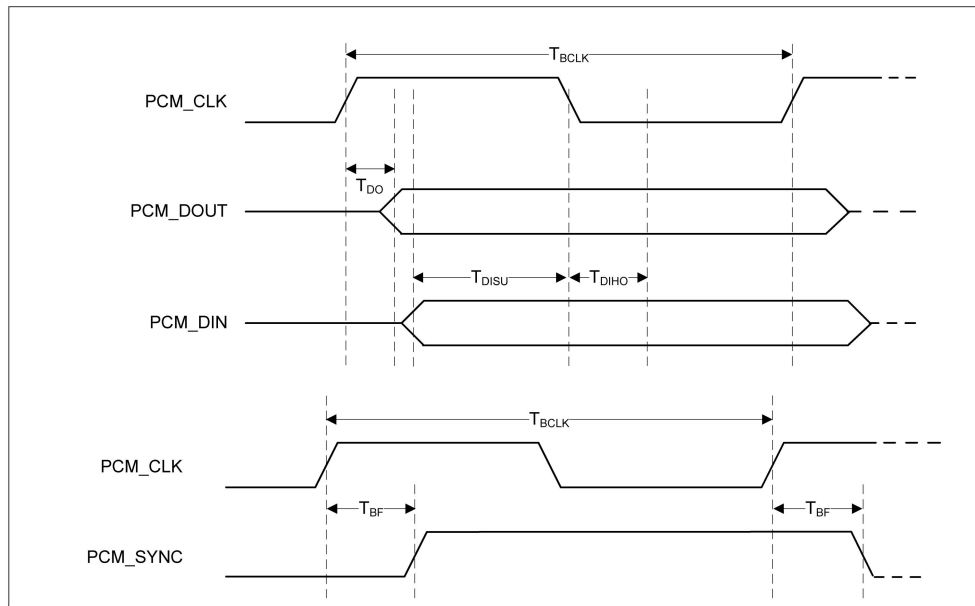
6.4.5 High-speed UART specifications



Symbol	Parameter	Condition	Min	Typ	Max	Unit
T_{BAUD}	Baud rate	38.4 MHz input clock	250	--	--	ns

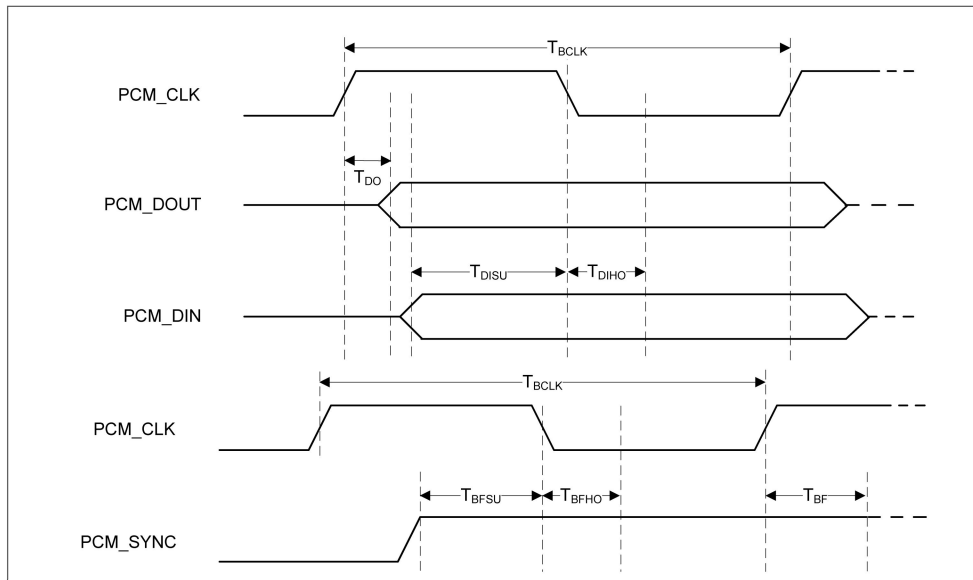
6.4.6 Bluetooth PCM Timing

Master Mode



Symbol	Parameter	Condition	Min	Typ	Max	Unit
F_{BCLK}	Bit clock frequency	--	--	2/2.048	--	MHz
Duty Cycle _{BCLK}	Bit clock duty cycle	--	0.4	0.5	0.6	--
$T_{BCLK \text{ rise/fall}}$	PCM_CLK rise/fall time	--	--	3	--	ns
T_{DO}	Delay from PCM_CLK rising edge to PCM_DOUT rising edge	--	--	--	15	ns
T_{DISU}	Setup time for PCM_DIN before PCM_CLK falling edge	--	20	--	--	ns
T_{DIHO}	Hold time for PCM_DIN after PCM_CLK falling edge	--	15	--	--	ns
T_{BF}	Delay from PCM_CLK rising edge to PCM_SYNC rising edge	--	--	--	15	ns

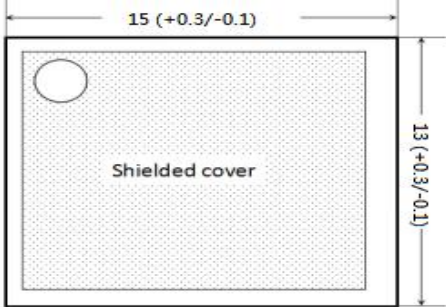
Slave mode



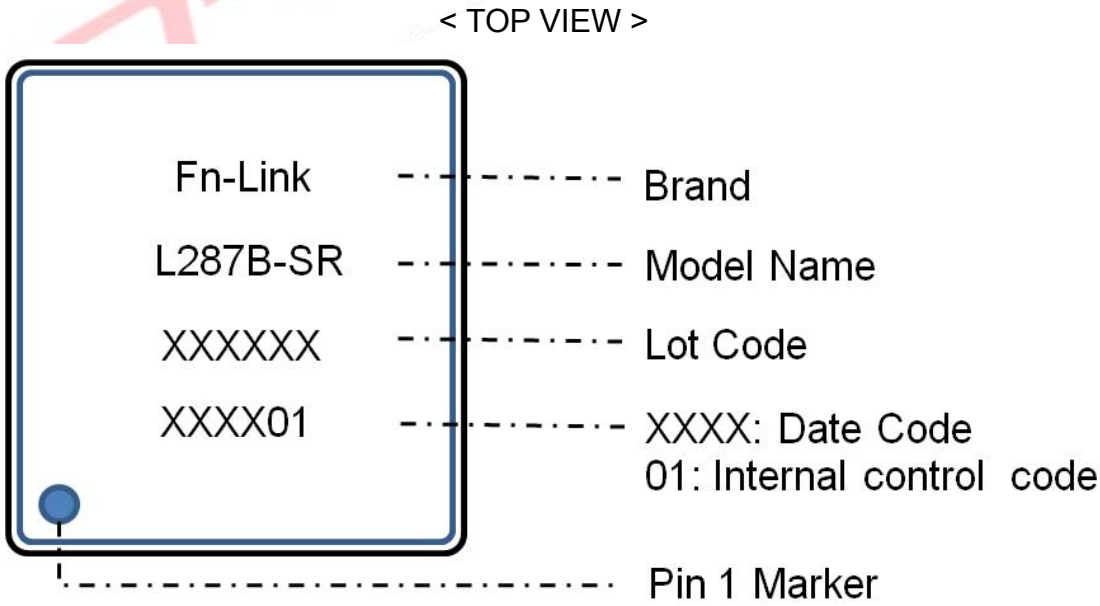
Symbol	Parameter	Condition	Min	Typ	Max	Unit
F_{BCLK}	Bit clock frequency	--	--	2/2.048	--	MHz
Duty Cycle _{BCLK}	Bit clock duty cycle	--	0.4	0.5	0.6	--
$T_{BCLK \text{ rise/fall}}$	PCM_CLK rise/fall time	--	--	3	--	ns
T_{DO}	Delay from PCM_CLK rising edge to PCM_DOUT rising edge	--	--	--	30	ns
T_{DISU}	Setup time for PCM_DIN before PCM_CLK falling edge	--	15	--	--	ns
T_{DIHO}	Hold time for PCM_DIN after PCM_CLK falling edge	--	10	--	--	ns
T_{BFSU}	Setup time for PCM_SYNC before PCM_CLK falling edge	--	15	--	--	ns
T_{BFHO}	Hold time for PCM_SYNC after PCM_CLK falling edge	--	10	--	--	ns

7. Size reference

7.1 Module Picture

L x W : 15 x 13 (+0.3/-0.1) mm 	
H: 2.15 (±0.2) mm	
Weight	0.855g

7.2 Marking Description

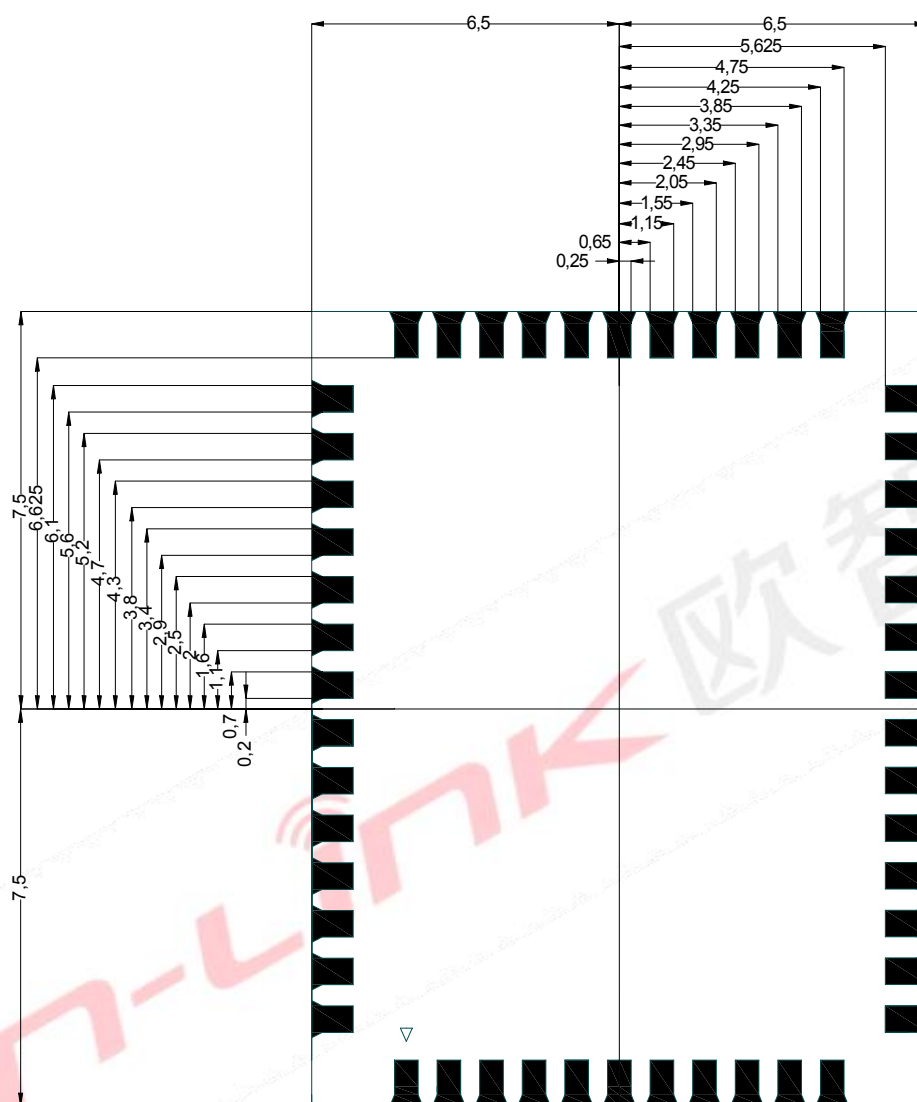


7.3 List of certified information

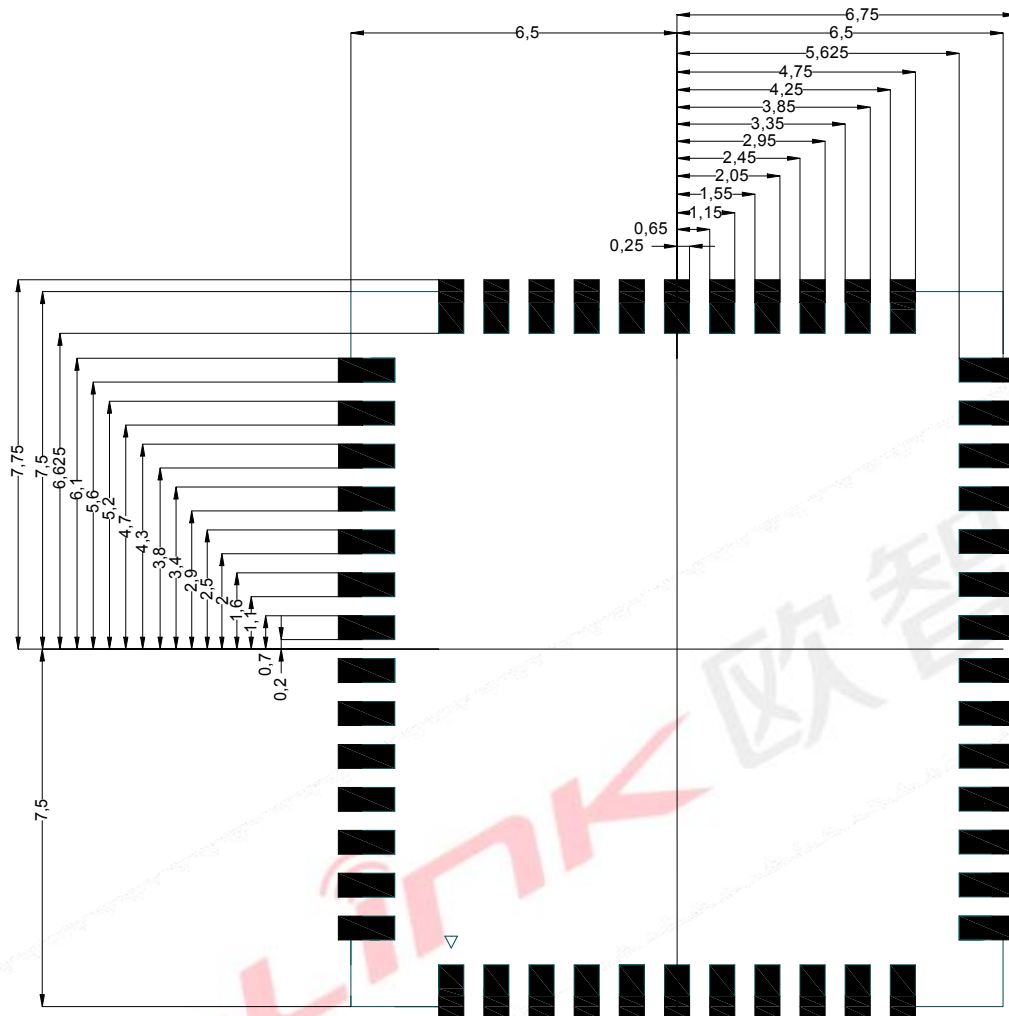
Certification project	Certificate number
SRRC	CMIIT ID:2022AP1095(M)
FCC	2AATL-L287B-SR
CE	1714-01-2022-116737
IC	TBD
NCC	TBD
KCC	TBD
TELEC	TBD
Brazil	TBD
Argentina	TBD
Japan	TBD

7.4 Physical Dimensions

<TOP View>



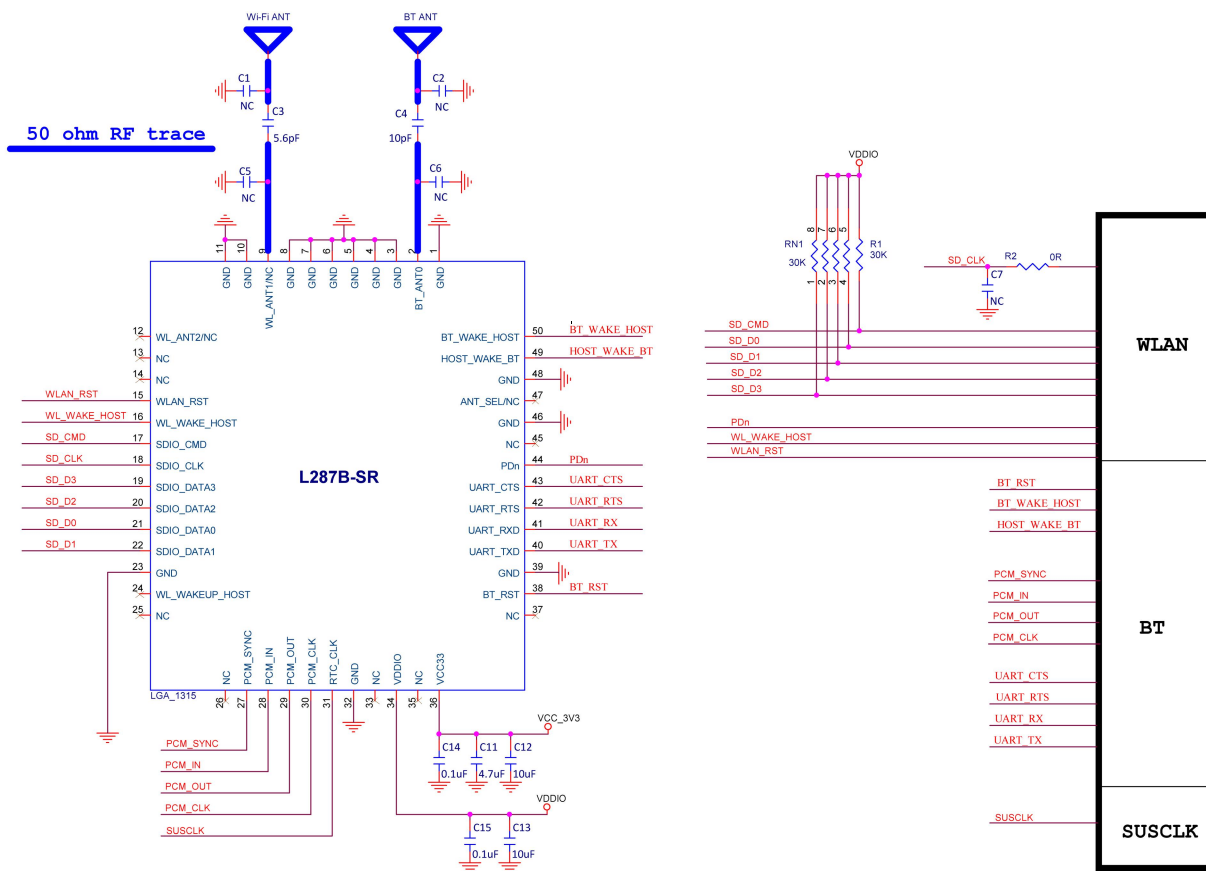
7.5 Layout Recommendation



8. The Key Material List

Item	Part Name	Description	Manufacturer
1	Inductor	2016 2.2uH, $\pm 20\%$	Sunlord, Ceaiya, Cenker, TAIYO YUDEN
2	Diplexer	1608 Dual-band, dual-mode 2.4GHz/5GHz WLAN	Glead, Walsin, ACX, Murata, MAG.LAYERS
3	Crystal	2016 38.4MHz	ECEC, TKD, Hosonic, JWT, TXC
4	Chipset	88W8987-A2-NYEE	NXP
5	PCB	FR4, GREEN	GDKX, Brain-power, Sunlord, Pirotek

9. Reference Design



C11, C12, C14 should be placed close to pin 36 of the module
C13, C15 should be placed close to pin 34 of the module

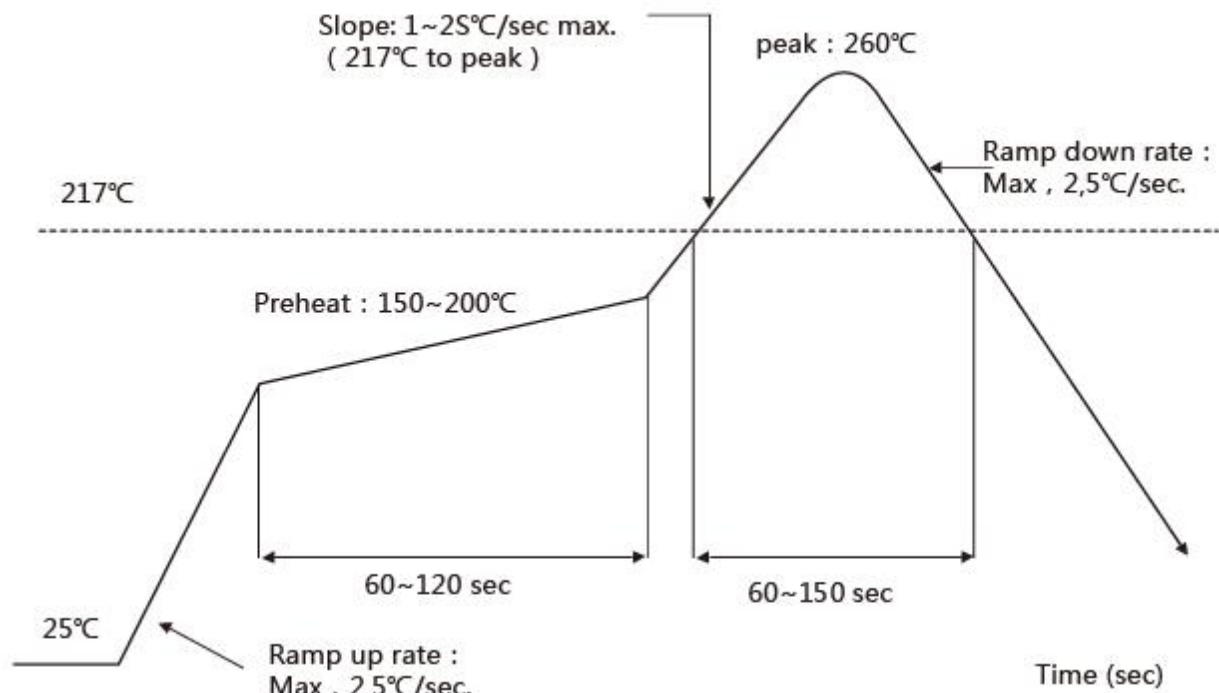
Module requires independent power supply with VCC_3V3 current $\geq 1\text{A}$. Do not share power with amplifier, infrared device, camera, etc. And please pay attention to the power up sequence requirements in part 6.3.

10. Recommended Reflow Profile

Referred to IPC/JEDEC standard.

Peak Temperature : $<260^{\circ}\text{C}$

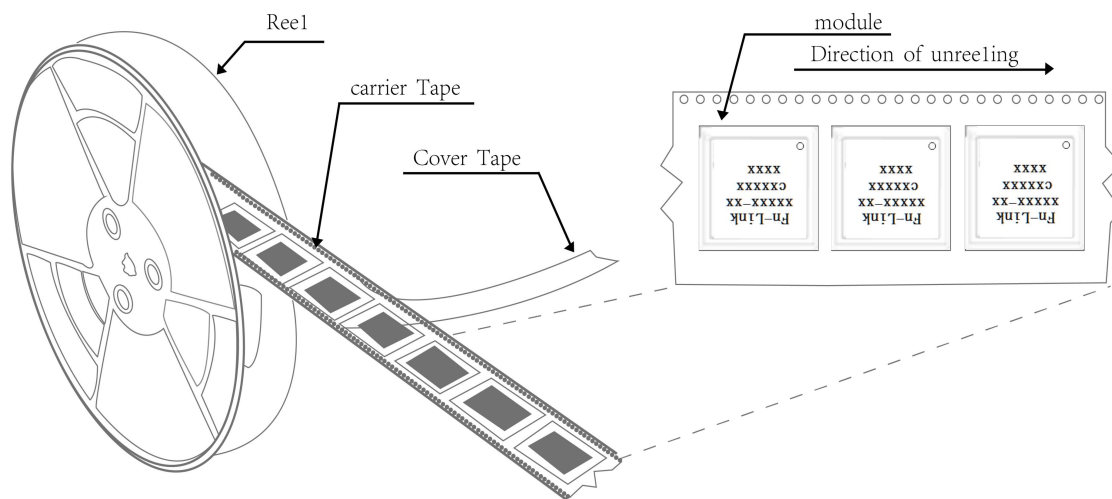
Number of Times : ≤ 2 times



11. Package

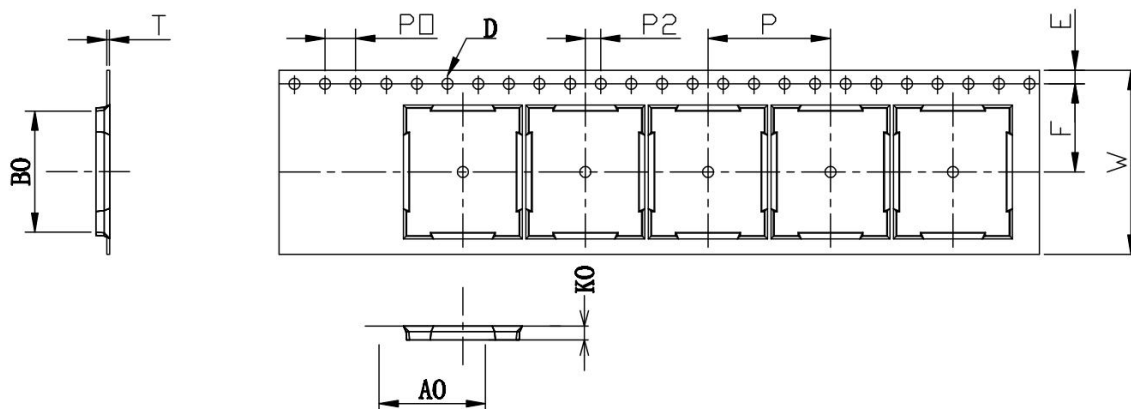
11.1 Reel

A roll of 1500pcs

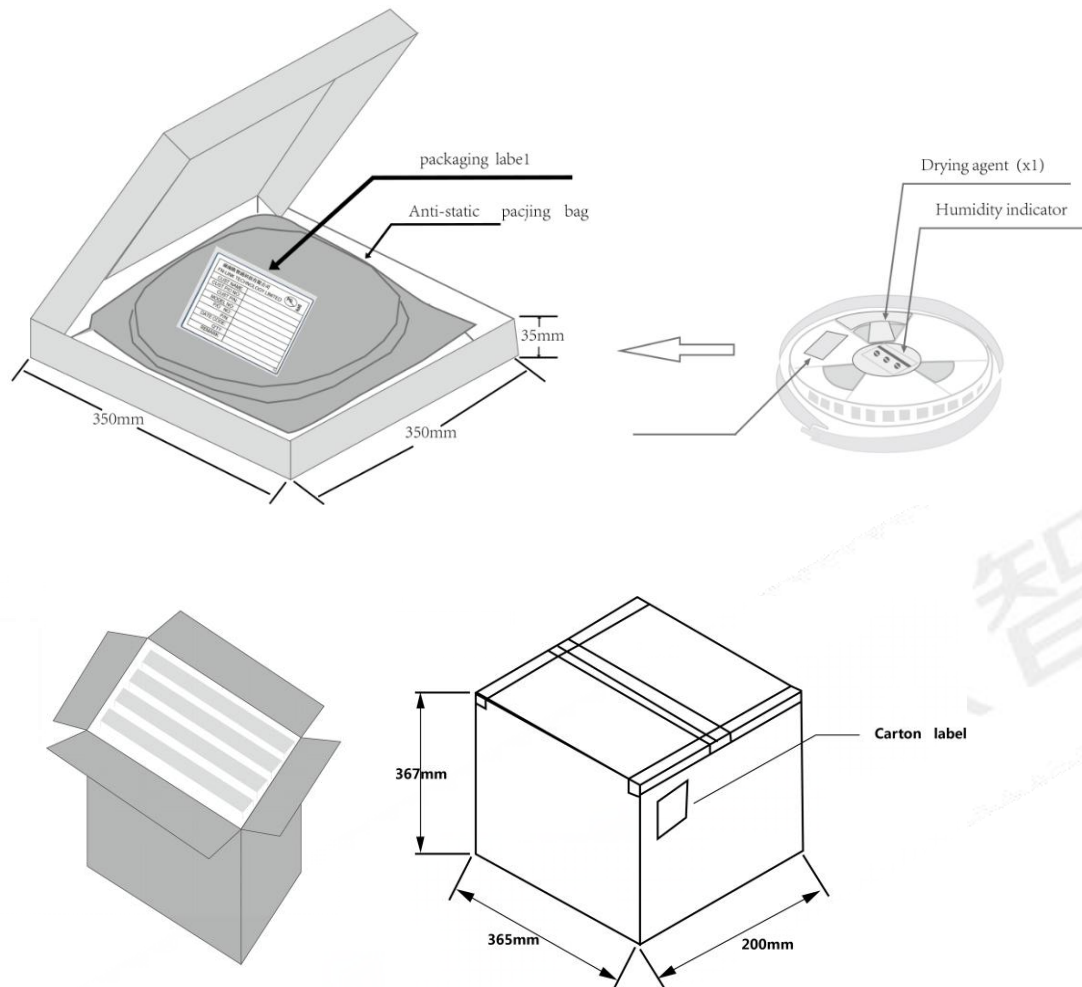


11.2 Carrier Tape Detail

ITEM	W	A0	B0	D	F	E	K0	P0	P2	P	T
DIM	24	13.40	15.40	1.50	11.5	1.75	2.65	4.0	2.0	16.0	0.30
TOLE	$\begin{smallmatrix} +0.3 \\ -0.3 \end{smallmatrix}$	± 0.15	± 0.15	$\begin{smallmatrix} +0.1 \\ -0.0 \end{smallmatrix}$	$\begin{smallmatrix} +0.1 \\ -0.1 \end{smallmatrix}$	± 0.1	± 0.10	± 0.1	± 0.1	± 0.1	± 0.05



11.3 Packaging Detail



12. Moisture sensitivity

The Modules is a Moisture Sensitive Device level 3, in according with standard IPC/JEDEC J-STD-020, take care

all the relatives requirements for using this kind of components.

Moreover, the customer has to take care of the following conditions:

- Calculated shelf life in sealed bag: 12 months at $<40^{\circ}\text{C}$ and $<90\%$ relative humidity (RH)
- Environmental condition during the production: 30°C / 60% RH according to IPC/JEDEC J-STD-033A paragraph 5

- c) The maximum time between the opening of the sealed bag and the reflow process must be 168 hours if condition
- d) "IPC/JEDEC J-STD-033A paragraph 5.2" is respected
- e) Baking is required if conditions b) or c) are not respected
- f) Baking is required if the humidity indicator inside the bag indicates 10% RH or more